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Linear Feedback Shift Register Based Test Vector Generation Using Sense Amplifier Based Flip Flop

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ABSTRACT
Digital systems performance is often governed by performance of flip flops and timing elements. Several Sense Amplifier based Flip Flops (SAFF) are reported in literature but they suffer with current contention and glitches. To overcome this, glitch free circuit is designed for Strollo's SAFF. This improved design has been successfully employed in four bit Linear Feedback Shift Register (LFSR). Further, these are implemented using 45nm technology. Simulation results validate the superiority of the proposed design to existing SAFFs in terms of average power consumption. Asynchronous single pulse is applied to the Strollo's SAFF with glitch free, resulting in a change in one output of four-bit LFSR. This is considered as a fault or test vector. The single stuck-at-fault method is used to correct the detected fault in the designed four-bit LFSR at the other end. This implementation is helpful in developing data protection circuits. .

Key words: CMOS Integrated Circuits, Flip-Flop, Four-bit LFSR, SAFF, Stuck at Fault.

1. INTRODUCTION

High speed with low power is a major aspect in design of digital circuits. Flip-flop (FF) is a fundamental building block of digital electronics systems like communications, computers and other electronic systems [1]. Delay and power of these basic storage elements defines performance and power of designed systems [2]. FF consumes a significant portion of the power of the digital system [3]. Further, setup-time influences the maximum clock of digital system. Hence, there is a requirement to optimize delay and power of FFs to improve the overall performance of digital systems.

The most regularly explored FF in digital systems is master–slave flip-flop (MSFF) [4]. Data has to pass through first latch before proper edge of clock, to capture correct data at proper edge of clock. Consequently, results in a comparatively long setup time in the MSFF. Pulse-triggered flip-flop (PFF) is reflected as one of the fast FFs. Typical PFF consists of a single latch and a clock pulse generator [5]. Major problem associated with PFF is deciding the pulse width of clock. A pulse width that is too narrow will not assure accuracy of captured data, although the hold time would be improved by a long pulse width. This is termed as sizing problem which limits its usage in various applications.

SAFF was first introduced [6], which is another fast FF with a negative set-up time. The SAFF is composed of a sense-amplifier (SA) stage and a slave latch, shown in Figure 1.

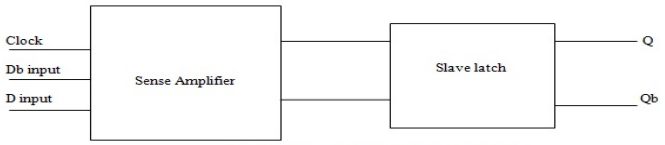

Figure.1 Block Diagram of Sense Amplifier Based Flip Flop

SA stage captures data right after rising edge of clock, and SA stage output is maintained during positive half cycle of clock. Consequently, sizing problem in PFF is addressed. As well, SAFF with negative setup time and decreased hold time can substitute MSFF. However, SAFF has some problems. SAFF pre-charge stage

consumes more power and delay involved in clock to q in the latch. Several SAFFs viz., Implemented SAFF [8], NAND based SAFF, Nikolic's SAFF, Kim's SAFF, and Strollo's SAFF are being implemented. In this work, initially various SAFFs are designed and implemented. An effort is made to design a glitch free circuit for Strollo's SAFF. Further, this improved Strollo's SAFF is used in the design of 4-bit LFSR. Rest of paper is organised as follows. Section 2 describes various SAFF; design methodology is exemplified in section 3. Section 4 discusses results and followed by concluding remarks in Sec 5.

2. SENSE AMPLIFIER BASED FLIP FLOPS

The SAFF has mainly two stages: first stage is sense amplifier and second stage is slave latch. Sense Amplifier stage is followed by slave stage. SA stage, whichever $\overline{r}$ or $\overline{s}$ becomes low then if and only if q and $\overline{q}$ are driven in slave stage according to state of $\overline{r}$ and $\overline{s}$. SA stage consists of internal nodes which are S and T, and it is when precharge voltage level is resulted by threshold voltage of NMOS transistor. In that time clock signal precharge phase becomes low. Hence, NMOS transistor is off condition and corresponding two PMOS transistors are on condition [1].

2.1 Implemented SAFF

The Implemented SAFF is able to be supplement of an isolation inverter and it is on condition of output and to develop another stage input of delay as shown in Figure.2. In that case, two different stages of delays are to produce low-to-high and high-to-low transitions [8]. After that it will remunerated because of slight asymmetrical inverter is used in implemented SAFF.

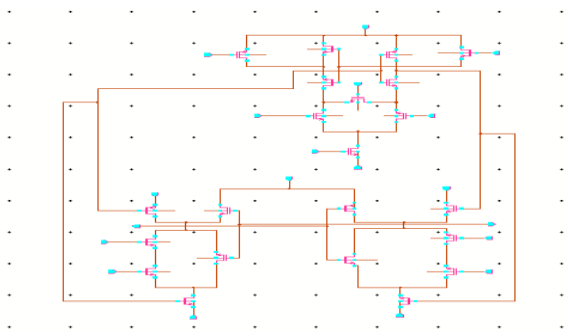

Figure.2 Implemented SAFF

2.2 Nand based SAFF

Nand based SAFF is composed of an inconsistency sense amplifier stage followed by a slave stage of Nand based reset-set is fairly unfettered by the aforesaid large setup time and the sizing difficulty [1]. Nand based SAFF in that when $\overline{r}$ change to low state irrespective of previous state of q or $\overline{q}$ condition, either high state or low state according to Nand based slave stage is $\overline{q}$ output is first change from high state and q change from low. During that will cause $\overline{r}$ is to be discharged more than $\overline{s}$, while $\overline{s}$ and $\overline{r}$ are *V*dd and *V*gnd respectively. Here, Nand based SAFF as shown in Figure.3. If the SA stage transition is to start from on/off state of two different PMOS transistors and only one NMOS transistor is on/off state. After that middle point is S and T is discharge with Vss voltage owing to NMOS transistor is connected to ground. The Nand based slave stage operation is slow because of q delay depends on $\overline{q}$ delay.

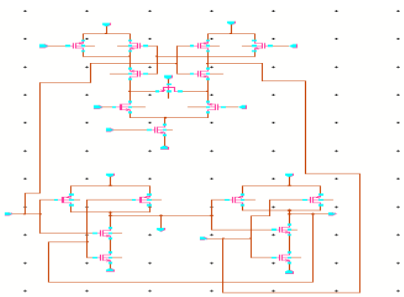

Figure.**3** Nand based SAFF

The main trouble of Nand based SAFF is more power dissipation and asymmetrical delay with high-to-low transitions with clock-to-output delay [9].

2.3 Nikolic's SAFF

The Nikolic proposed a SAFF as shown in Figure.4. In this structure, r and s signals are to be generated and when the use of two inverters is to control the output nodes are q and $\overline{q}$ respectively [8]. Therefore, the speed of measure is to be consideration of high-to-low transition of q ($\overline{q}$) is firm as a result of fast r (s) rise in the SA stage, which means that the delay of q is independent of the $\overline{q}$ (q) delay [10].

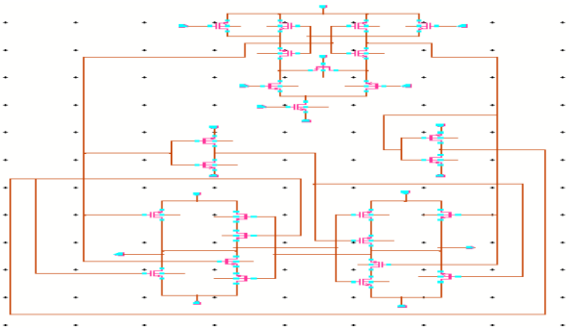

Figure.4 NIKOLIC's SAFF

2.4 Kim's SAFF

The Kim's developed SAFF as shown in Figure.5 which provides flatten path for q ($\overline{q}$), and also grant the $\overline{q}$ (q) is convenient alone. The Kim's SAFF is a glitch frequency is appear on output nodes q and $\overline{q}$ outputs are independent of past state of q and $\overline{q}$ and D is set to high. When the clock is going to high state, q must be high, because $\overline{s}$ has not discharge via SA stage is to drive through flatten path of q and two of NMOS transistors are enabled. The glitch frequency is enabled at node of q caused by $\overline{s}$ is fully discharged and immediately when clock is going to high. All though discharging path $\overline{s}$ is the lengthy process. At the clock is going to high discharge path of $\overline{s}$ in the SA stage is driven because of pre-charge $\overline{r}$ is decrease from *V*dd.

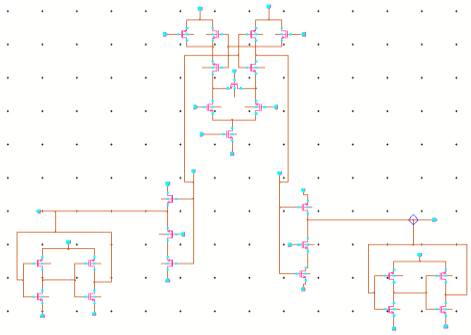

Figure.5 KIM's SAFF

The Nikolic proposed SAFF is improved version of Nand based SAFF while using a symmetrical two-Inverters of Slave Stage and both composite CMOS gates [11]. The performance increase is rewarded and also additional number of transistors present in the output stage is to be considered [1]. The Kim proposed SAFF slave stage is realized with two NCMOS transistors and two cross-coupled pathetic inverters are required to stand on flip-flop is static [12]. The Kim SAFF is especially high-speed compare to previous SAFF, output diminishing logic is a solitary delay of gate with respect to the leading edge of clock, and 14 MOS transistors are required [13]. The motive of SAFF is regarded as proper preference for small V_{dd} application. Basically SAFF suffer from two main crises in low voltage surroundings [14]. The first problem is the added glitch frequency appeared at output nodes, and is precise for less weight conditions. The second problem is the use of cross-couple inverters and also tune to an appropriate transistor sizing and it will suffer from crow bar current then it will increase power dissipation. This glitch problem is being addressed in this work and is detailed in the next section.

3. DESIGN AND METHODOLOGY

Various SAFFs that are discussed in the previous section are designed and implemented using gpdk45nm technology. The strollo's SAFF produces the relative outputs compared to other SAFF's, but it has some glitch frequency in it. The glitch free circuit is designed for strollo's SAFF to avoid glitch frequency in it.

3.1 Strollo's SAFF

The Strollo's recommended a SAFF as shown in Figure.6. It is a combination of Kim's design and Nand based SAFF. It overcomes the previous SAFF limitations in the Strollo's SAFF that is some glitch frequency in it. In addition to avoid glitch frequency problem in Strollo's SAFF with glitch free circuit used, the contention of current flows through output nodes q and $\overline{q}$ appeared in previous SAFF. Removing glitch free circuit is in-built two cross-coupled inverters and some of pass-transistors. The Kim's SAFF compare to strollo's SAFF found large glitch frequency is formed and it will expand the pull-down path, does not remove the current contention.

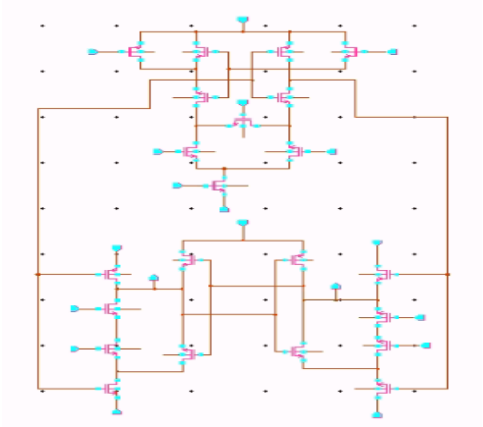

Figure.6 STROLLO's SAFF

3.2 Glitch Free Circuit

A glitch free circuit method is that equally glitch eradicates on sinusoidal signal has when an input signal include delay circuit or a glitch free circuit or a latch circuit. For example the delay circuit is receives the input signal and to introduces a delay into it. This operation is as shown in below figure.7.

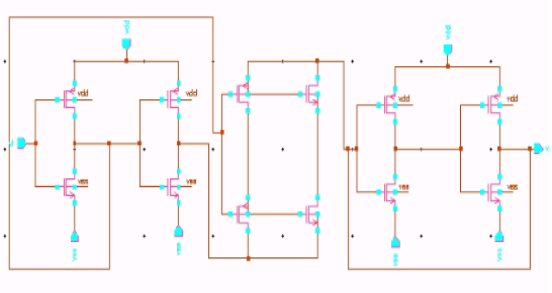

Figure.7 (a) Schematic

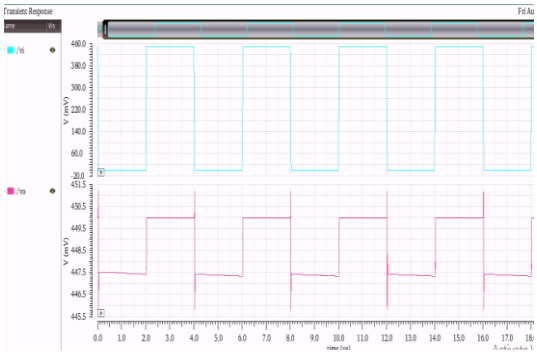

Figure.7 (b) Waveforms

3.3 Strollo's SAFF with glitch Free

The Stollo's SAFF is benefit with compared to previous SAFFs and while Stollo's SAFF output nodes q and $\bar{q}$ glitch removed by using removing glitch frequency circuit shown below figure.8.

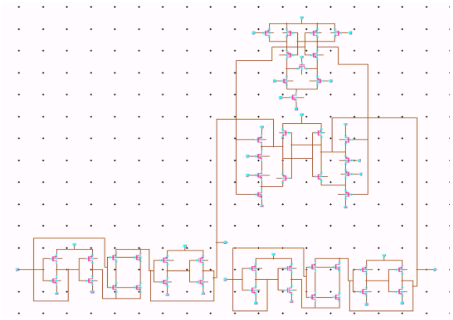

Figure.8 STROLLO's SAFF with Glitch Free

3.4. Four–Bit LFSR Using Strollo's SAFF with glitch free Circuit

The basic function of conventional LFSR is to generate sequence based on clock and D input signals [15].Four-Bit LFSR is designed using strollo's SAFF with glitch free. Further, asynchronous pulse is applied to reset pin after that one selected output bit is potentially changed or the distorted is called test vector, and the changed bits or test vectors are perform XOR operation. Asynchronous pulse property is not available in conventional four bit LFSR using Boolean logic flip flops.

The block diagram of the four bit LFSR using strollo's SAFF with glitch free as shown in below figure.9

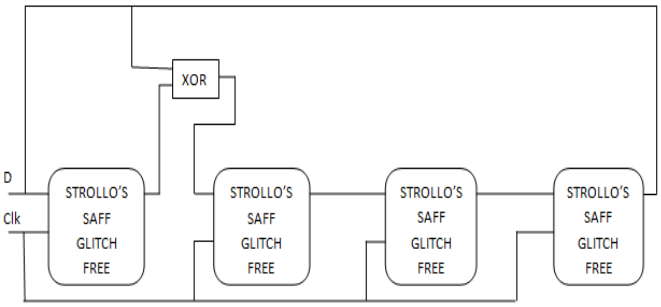

Figure.9 Block Diagram of Four- bit linear feedback circuit using STROLLO's SAFF with glitch free

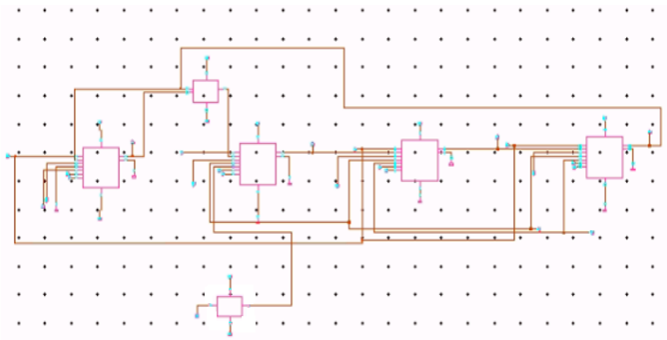

Figure.10 Four bit linear feedback circuit using STROLLO's SAFF with glitch free circuit Schematic

- Four bit LFSR polynomial considered in this design is x^4+x+1.
- Leftmost bit decides whether the for example "XXXXX" xor pattern is used to compute the next value or if the register just shifts left. If more flip-flops needed, then more xor gates needed.

3.5 Single stuck-at-fault method

Designed Four-bit LFSR four outputs q0, q1, q2, q3 of one selected output q3 is considered as fault output, that fault is connected to stuck at zero/ stuck at one to recollect the original output and remaining all outputs are remains constant. The Four-bit LFSR is connected to stuck at fault circuit as shown in below figure.11

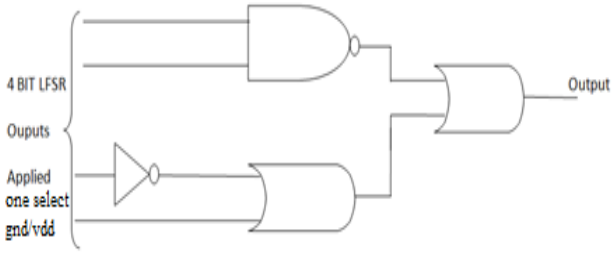

Figure.11 Single stuck at fault Block Diagram

- Single stuck at zero/one logic network of Boolean gates are and, or, not, nand.
- One line has set either 0 or 1 value free of other signal value.
- Single split up branch can be stuck most ordinary representation for Boolean analysis.

3.5.1. Implementation of Four -Bit LFSR Using STROLLO's SAFF with Glitch Free circuit through Single Stuck at Zero

One output of Four-bit LFSR using Strollo's SAFF has single fault that will be correction is necessary and is corrected by using single stuck at fault method as shown in belowfigure.12.

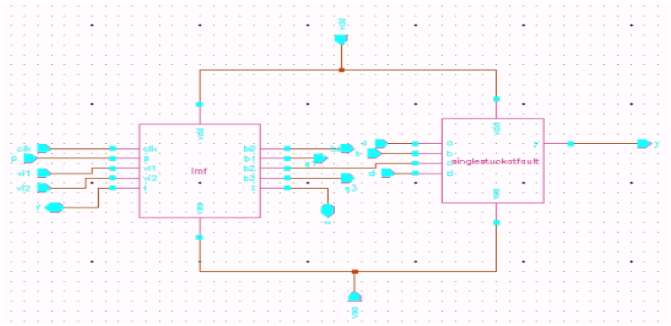

Figure.12 Four-bit LFSR Using STROLLO's SAF with Glitch Free through Single Stuck at Zero Schematic

4. RESULTS AND DISCUSSIONS

Various SAFFs that are discussed in the previous section are implemented using 45nm Cadence virtuoso technology. Glitch free circuit and 4-bit LFSR are also implemented with the same technology. Simulation results obtained from various types of SAFF's viz., Implemented SAFF, Nand based SAFF, Nikolic's SAFF, Kim's SAFF, Strollo's SAFF and Strollo's SAFF are shown in Figures 13 to 19.

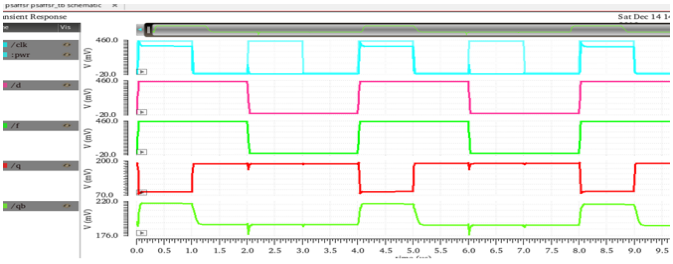

Figure.13 Implemented SAFF

The figure.13 shows that simulation of Implemented SAFF is same configuration of inputs are applied but received output configuration is different in nature. It has narrow width logic low, long propagation delay with logic high. It has less average power.

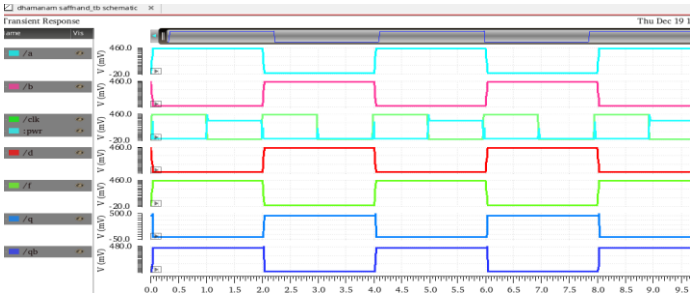

Figure.14 NAND Based SAFF

The figure.14 indicates simulation of NAND Based SAFF is applied different configuration of inputs and to getting outputs q and $\bar{q}$ are taken from two cross coupled NAND gates with high power dissipation.

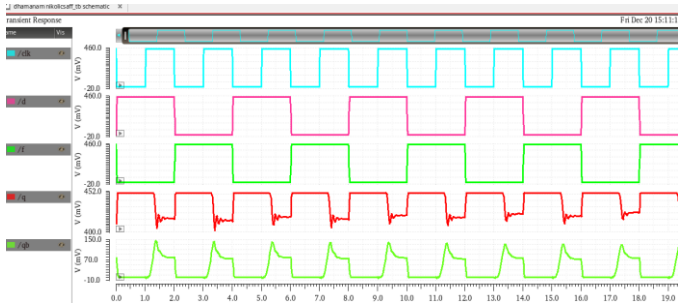

Figure.15 NIKOLIC'SSAFF

The figure.15exhibit simulation of Nikolic's SAFF is improper glitch appeared in outputs q and $\bar{q}$.

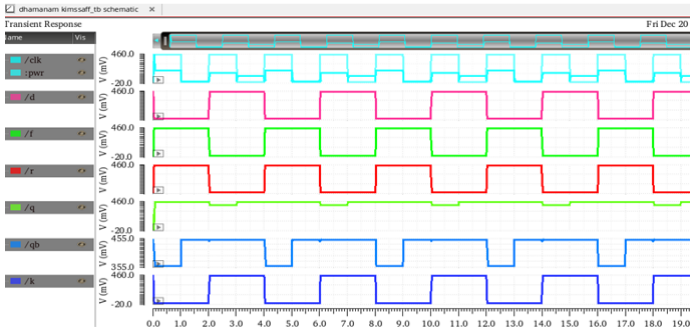

Figure.16 KIM'SSAFF

The figure.16 shows simulation of Kim's SAFF is one output q is logic high constant with some flatten glitch and $\bar{q}$ output is small amount of logic low with low propagation delay.

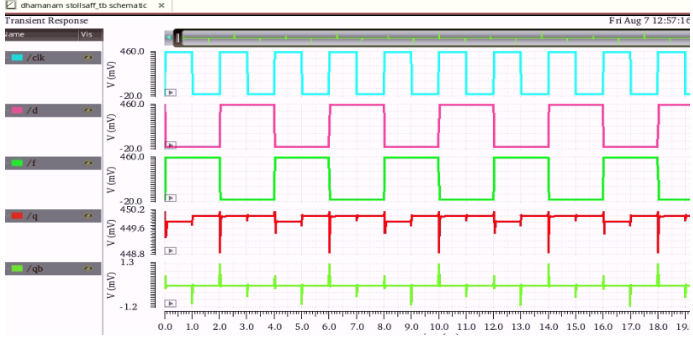

Figure.17 STROLLO'S SAFF

The figure.17shows simulation of STROLLO'SSAFF, its outputs q and $\overline{q}$ are high amount of glitch appeared but it has less average power and less time delay. With regard to these parameters it is the most convenient SAFF.

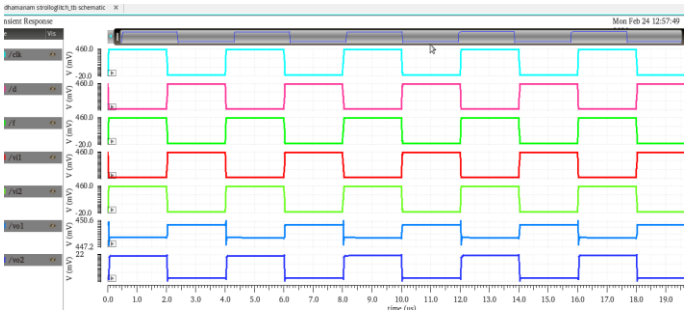

Figure.18 STROLLO'S SAFF with glitch free

The figure.18 exhibit simulation of Strollo's SAFF with glitch free, output of previous strollo's SAFF q and $\overline{q}$ is also same but it does not have glitch frequency.

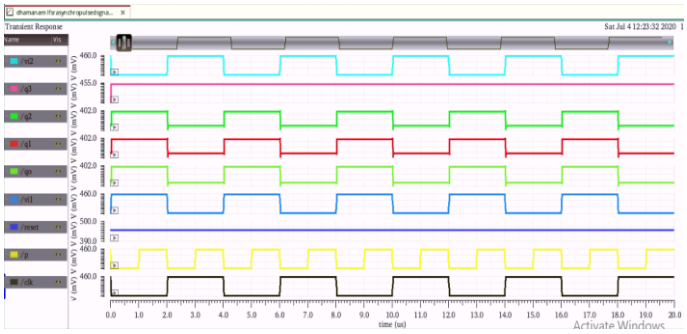

Figure.19 Four bit linear feedback using STROLLO'SSAFF with glitch free

The figure.19 shows simulation of Four bit linear feedback circuit and asynchronous single pulse is applied at reset pin is to make a disturbance in output is shown in output signal q3.

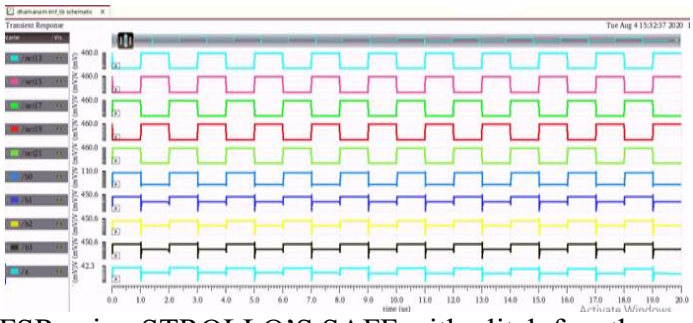

Figure.20 Four bit LFSR using STROLLO'S SAFF with glitch free through single stuck at zero

The figure.20 shows simulation of 4 bit LFSR with single stuck at zero is recovered from Four bit linear feedback using Strollo's SAFF with glitch free fault signal in it.

Table.1.shows the performance comparison of different types of SAFF's using cadence virtuoso gpdk45nm technology.

Table.1: Comparison of Different types of SAFF.

	AVERAGE POWER	TIME DELAY	AREA
IMPLEMENTED SAFF	4.450E-^{9}	1.816E-^{6}	13.1044
NAND BASED SAFF	8.078E-^{9}	2.040E-^{6}	10.8241
NIKOLIC'S SAFF	828.3E-^{12}	1.999E-^{6}	15.5630
KIM'S SAFF	225.0E-^{3}	1.960E-^{6}	14.4020
STROLLO'S SAFF	320.5E-^{12}	2.044E-^{6}	13.1769
STROLLO'S SAFF WITH GLITCH FREE	240.0E-^{3}	2.049E-^{6}	27.5100

It is evident from above table that strollo's SAFF performance is better than other SAFFs in terms of average power consumption. Delay and area are comparatively a bit high when compared with other SAFFs.

5. CONCLUSION

Various types of SAFF's are implemented using cadence virtuoso gpdk45 technology. The glitch frequency problem in Strollo's SAFF is addressed with the design of glitch free circuit. A four bit LFSR is designed with this improved Strollo's SAFF. The designed 4 bit linear feedback shift register operation is done after that one fault output is occurred and it is corrected through single stuck at fault method. All these designs are being implemented in 45nm technology using Cadence virtuoso tool. Simulation results indicate that this improved Strollo's SAFF is better in terms of average power consumption. However, the glitch free Strollo's SAFF suffers from comparatively more delay and area. This can be addressed in our future work by reducing delay involved from clock to output of the latch.

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