European Journal of Molecular & Clinical Medicine
ISSN 2515-8260 Volume 07, Issue 08, 2020

# An Efficient Denoising Architecture of MVD-RCA-SP-FIR filter for Real-time ECG signals

Yalamanchili Arpitha[1], Dr G. L. Madhumathi[2], Dr N. Balaji[3]

*[1]Associate Professor, Department of ECE, NRI Institute of Technology, Pothavarappadu-521212, Andhra Pradesh, India*
*[2]Professor & HOD, Department of ECE, Dhanekula Institute of Engineering and Technology, Ganguru-Andhra Pradesh, India*
*[3]Professor, Department of ECE, JNTUK university, Kakinada, Andhra Pradesh, India*

*Emal: [1]yalamanchiliarpitha@gmail.com, [2]madhumati70@rediffmail.com, [3]narayanam.b@rediffmail.com*

***Abstract- Electrocardiogram (ECG) is non-stationary, non-periodic real-time signal. It is provided to use full electrical information about heart functioning. It means by the analysis of ECG signal; we can identify any living person's hearts are working properly or not. In recent years there is a huge demand for the reduction of size and power of portable devices used for monitoring critical signals such as ECG. The technical advancements in VLSI have created a huge impact on biomedical signal processing. VLSI circuits working at high speed and these can be designed to consume less area and power. Especially for ECG signal denoising, digital filters such as FIR and IIR are used in most of the applications. Finite Impulse Filters (FIR) are used widely compared to IIR filters because of their good stability and high order. In this paper, FIR filter with modified Vedic multiplier-based architecture is introduced to carry out ECG signal denoising application. In this paper at first resource-efficient Vedic multiplier is introduced which is around 55% area-efficient for 8 bit, 15% efficient in terms of delay, and 45% efficient in terms of power in comparisons of the latest design proposed in 2020. Then with the help of a modified Vedic multiplier, FIR is developed which is also efficient in terms of resources. It has 40.5% better ADP and around 20% better APP. This latest design of the filter is much helpful for ECG signal denoising.***

***Keywords: Cardiovascular Diseases (CVD)Electrocardiogram (ECG), Denoise, Finite Impulse Response (FIR), Multiply Accumulate***

## I. INTRODUCTION

Electrocardiogram (ECG) is non-stationary, non-periodic real-time signal. It is provided to use full electrical information about heart functioning means by the analysis of ECG signal, we can identify any living person's hearts is working properly or not [1-2]. Nowadays, ECG is used as a diagnostic tool for various diseases like Chronic patient surveillance, Physiological feedback, Sleep apnea, Arrhythmias, Emotional and physical activity recognition systems arrhythmia [3-11]. It also indicates all of the Cardiovascular Diseases (CVD)like Sudden chest pain, Chances of cardiac arrest, and sometimes reporteddeath also due to cardiac attack [12].ECG signal waveform is shown in Fig. 1. Till noise detection and denoise ECG signal are a big challenge for the researcher because ECG diagnosis is depending on ECG signal quality [13-14]. The block representation of ECG signal denoising

is shown in Fig. 2. Many studies have been done by researchers on ECG denoising. As we are aware that a linear system is used

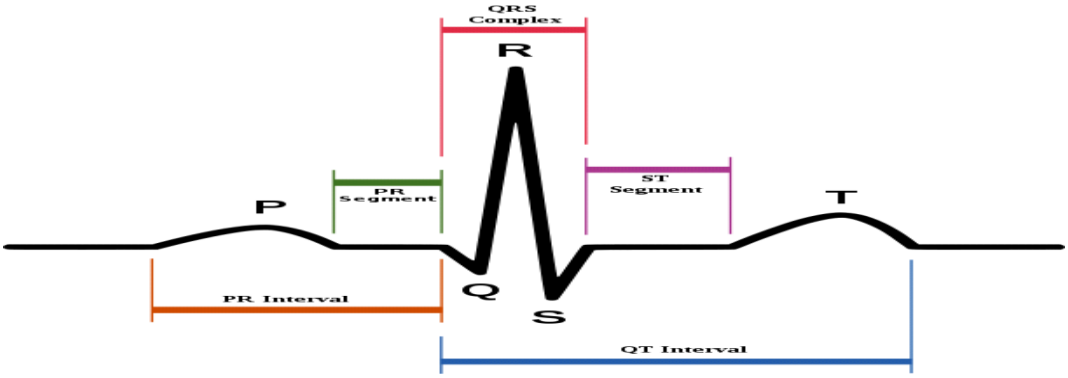



Fig. 1:ECG Signal Waveform

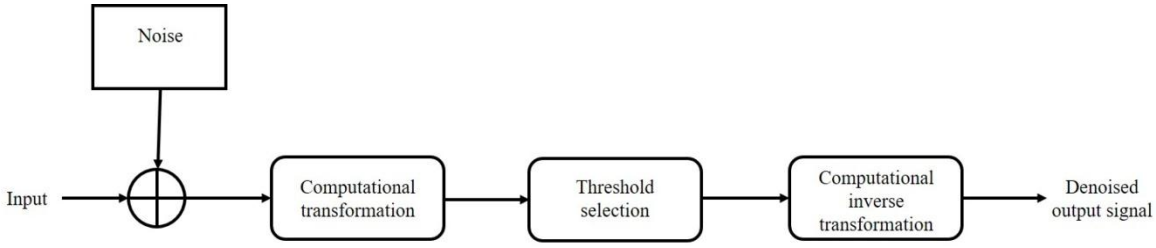



Fig. 2: Block diagram of ECG Signal Waveform denoising

for noise removal for signals. Most digital filters are used as a linear system so it is frequently used for denoising ECG input signals [14-15].

ECG signals mainly contain four types of noises [16].

1). Baseline wander,

2). Electrode motion artifact noise,

3). Electromyographic (EMG) noise,

4). Powerline interference

For easy understanding of the various type of noises and appropriate method of removal, here one by one we are discussing the type of noises and which types of the digital filter is most suitable for noise removal. Baseline wander is also frequently calling as a baseline draft [17]. This type of noise gets due to patient movement and breathing. That entire signal is the shift from the base X-axis. A Low-frequency signal around 0.5 Hz range frequency content is the reason for such type of ECG noise. For removal of baseline wander Finite Impulse Response (FIR) is most suitable.Electrode motion artifact noise occurs in the range of 1 to 10 Hz caused by skin stretching. EMG noise is created due to muscle noise, suppose required during exercise time [18]. Muscle noise is, in contrast to baseline wander and 50/60 Hz interference, not removed by narrowband filtering. Power line interference is the most common noise ECG signal. It is characterized by 50 or 60 Hz sinusoidal interference.

In recent years, in most of the signal processing applications, the FIR filter is used as a major building block. These filters are designed to obtain almost any type of digital frequency

response. The N-length FIR filter is designed with multipliers, adders and a series of delays to create the output of the filter. The delays operate on input samples and the value of the coefficients is used for multiplication. So, the output of the filter is the summation of all the samples that are delayed multiplied by appropriate coefficients.

This research paper is organized as follows: In section 2, we representthe systematic growth of the FIR filter in the field of anECG signal denoising. literature survey of recent papers based on the FIR filter. In section 3, we define the problem statement. In section 4 explained the proposed FIR filters design is presented. Section 5 gives the comparative experimental result of a proposed RCA-FIR. The conclusion is made in section 6.

## II. LITERATURE REVIEW

Generally, the FIR filter is implemented in the transposed direct form [1]. Multiplier plays a key role in FIR filter design. To perform the filter operation, the overall architecture of the FIR filter requires more area as it contains more multipliers. So, for FIR filter design the most important task is to reduce the area of multipliers [3]. To design the FIR filter usually MAC (Multiply and Accumulate) units are used. MAC units can be optimized for power and timing as proposed in [2]. For real-time ECG signals, the FIR based MAC units are used to suppress the power line interference (PLI) noise. The performance of the FIR filter depends on the speed of the MAC unit employed inside the filter. Various windowing methods for FIR filters such as Rectangular, Hanning, Kaiser, and Blackman windows have been proposed earlier. At the expense of high computational load and as the order of the filter is large, Kaiser and rectangular windows have shown better results. Among the various windowing methods discussed above, the FIR Kaiser Window filter provides better performance [4]. But an FIR filter with a MAC unit gives better performance in terms of power, area, and speed. Digital filter implementation in FPGAs and other VLSI implementations allow higher sampling rates and reduced cost than traditional DSP chips. Moreover, digital filters are extensively used because they have the potential to attain a much better signal to noise ratio than analog filters. Several methods of FIR architectures have been proposed earlier. In 2012, Tsao and Chao proposed parallel FIR filter architecture for symmetric convolution for odd length. It had a significant advantage in terms of hardware cost [19]. In 2013, park et al. proposed an adaptive FIR filter by using Distributed Arithmetic (DA) inner product computation and claim novel pipelined architecture for FIR filter as well as low throughput and efficient hardware [20].In at same year, martin Kumm proposed DA + Look-up Table (LUT) reduction technique based on reconfigurable FIR filter. It consumed less area in comparison to fixed DA [21].In the year 2014, park and Meherproposed new architecture of FIR filter with reconfiguration feature and whose filter coefficients get change during runtime [22]. In the year 2015, Ramandeep Kaur et al. proposed MAC based FIR filter architecture to minimize PLI noise [23]. In 2017, JiajiaChenet al. proposed a new algorithm for synthesizing finite precision coefficients of linear phase FIR filter [24]. In the same year, Durgesh Nandan et al. proposed logarithm multiplier-based FIR filter architecture forefficient hardware but this design get a compromise with accuracy [25]. In 2018, M. Sumalatha proposed efficient architecture of the FIR filter by using radix-8 based CLA [26]. In 2019, the same team of researchers proposed efficient architecture of the FIR filter for ECG denoising by using the Vedic multiplier and CLA [27]. In 2020, T.V.padmavanthy et al. improved performance for the FIR filter by using partial product separation of the Vedic multiplier [28]. In 2020, Rohini et al. provide FIR filter-based review papers in which she tries to summarize the entire FIR filter literature [29]. But still, there is scope to improved FIR filter design and make it hardware cost-efficient. In section 3, we identify the limitation of the literature and problem statement of this paper.

*Problem Statement*

In this section, we focus on the limitations of the existing designof the FIR filter. Although many researchers suggested various changes and try to make FIR filter architecture efficient there is always scope to make architecture more hardware efficient. Here, we address limitations of the FIR filter as well as show how the proposed design is overcome literature-based FIR filters.The concerns of FIR filter architecture are as follows.

1) The multiplier is the most area consuming component in the FIR filter. If the multiplier is less hardware efficient then FIR filter architecture has a less efficient design.
2) Adder design also plays an important role to make FIR filter architecture efficient.
3) An efficient pipeline process also plays an important role to make FIR filter hardware efficient.

Solutions: to overcome these limitations of FIR filter design, a Seamless pipeline-based FIR filter by using modified Vedic multiplier and RCA (MVD-RCA-SP-FIR) is used to developed hardware efficient FIR filter architecture. The Modified Vedic Multiplier (MVD) with partial product generation for the higher-order multiplier is used for optimized architecture for the Vedic multiplier which is based on the "Urdhava Triyakbhagyam" Vedic sutra. After working on component optimization, we applied seamless pipeline techniques for the equalization of components it minimized delay. This MVD-RCA-SP-FIR architecture helps to perform the ECG denoising application.

*Proposed work*

The overall block diagram for the ECG signal denoising various steps is shown in Figure 3. In this entire process at first, we put the ECG signal and add some noise then convert it in form of binary. After this write it in text format and pass it to the proposed MVD-RCA-SP-FIR filter. This paper mainly focused on hardware efficient MVD-RCA-SP-FIR filter architecture, the rest of the process is the same as previous literature. After then Fir filter output converted into text format and read signal via MATLAB. At last denoised ECG signal and calculated various parameters like SNR, BER, MSE, etc.

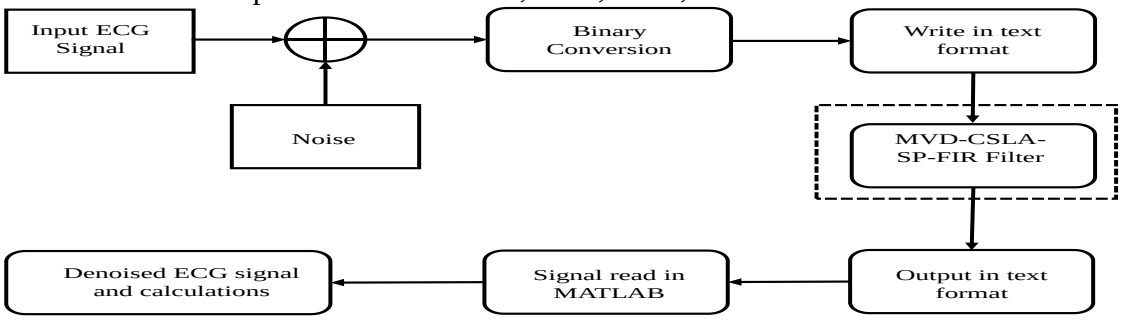



Fig 3: Overall Block diagram

The generalized equation of multi-tap Fir filter design is as shown below**,**

$$y(n) = \sum_{k=0}^{M-1} h(k)\, x(n-k) \quad (1)$$

Wherey(n),x(n) and h(n) are the output signal, input signal, impulse response respectively.

In the design of the FIR filter, major hardware building blocks are multiplier, adder, and delay circuits. Out of them, the multiplier is the most hardware consuming block. Many multipliers exist in the literature, everyone has its benefits and limitations [30-32]. The speed of multiplication of the process can be improved by the nature of the multiplier combing

Vedic mathematics. "Urdhva Tiryagbhyam" (vertical and cross-wise algorithm) forms the basis for this multiplier architecture[33]. Fig. 4, Reveals sutra "Urdhva Tiryagbhyam".

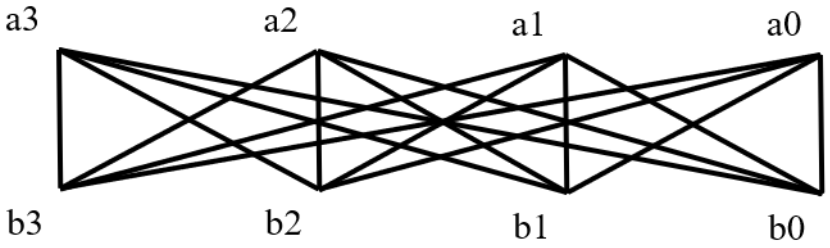



Fig. 4: Reveal's sutra "Urdhva Tiryagbhyam"

In a single “Urdhva Tiryagbhyam” sutra line, 4×4 multiplications can be performed [34]. However, to yield results, the move involves adding four partial items and adding a conventional technique. The steps taken by Urdhva Tiryagbhyam Sutra to calculate the final product in binary multiplication will be reduced. This intern increases multiplier speed and computational time decreases.

In this paper, we proposed a hardware efficient Modified Vedic Multiplier (MVD) by using Customized Hybrid Adder (CHA). By using MVD and Ripple Carry Adder (RCA), we developed the efficient architecture of the FIR filter. At last, we used Seamless pipelining [35] for enhancing the delay performance of our proposed FIR filter. Hardware efficient architecture of the FIR filter is much use full for ECG signal denoising.

1.1.4 × 4 Modified Vedic Multiplier (MVD) design algorithm

Fig. 5 shows 4×4 MVD multiplier by using 2×2 vedic multiplier and customized hybrid adder. The design proposed by Sumalatha et al. in 2019 and Padmavathy et al. in 2020 was not hardware efficient. For making 4×4 Vedic multiplier most efficient and resourceful

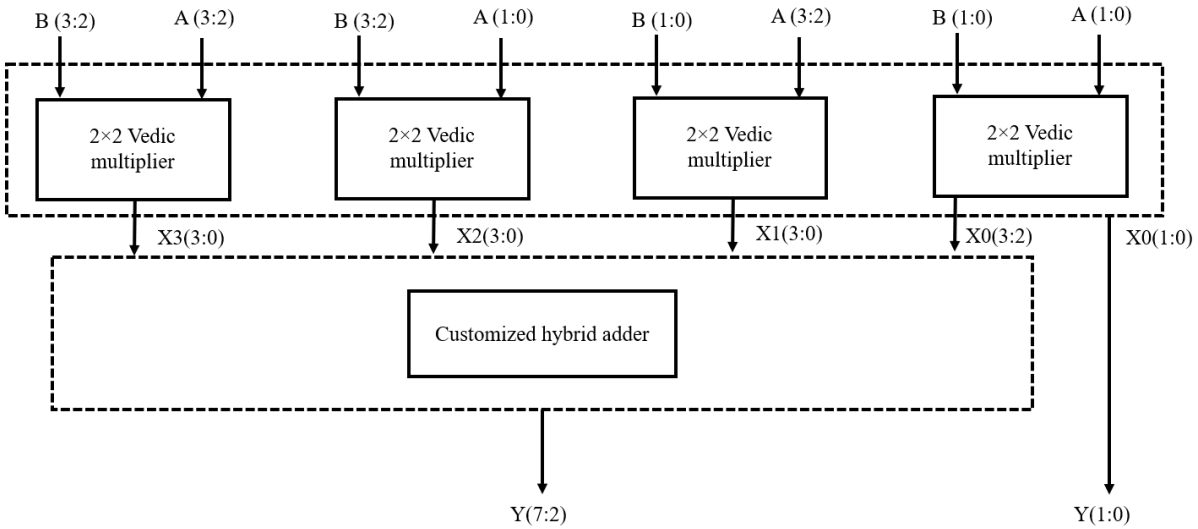



Fig. 5: 4×4 Modified Vedic Multiplier (MVD) block diagram

component, it proposed a CHA architecture that is used in the vedic multiplier as a component. CHA hardware architecture is shown in fig. 6. According to this diagram, VHDL coding is performed. CHA is mainly a mixed form of carrying Save Adder (CSA) and RCA.

After then according to circuit requirements, it gets customized for the best hardware requirements. CHA performed addition of 4 numbers out of the 3 numbers are 4-bit numbers and one number having 2-bit only. CHA architecture had used 6 full adders, 4 half adders and 2 xor gate.

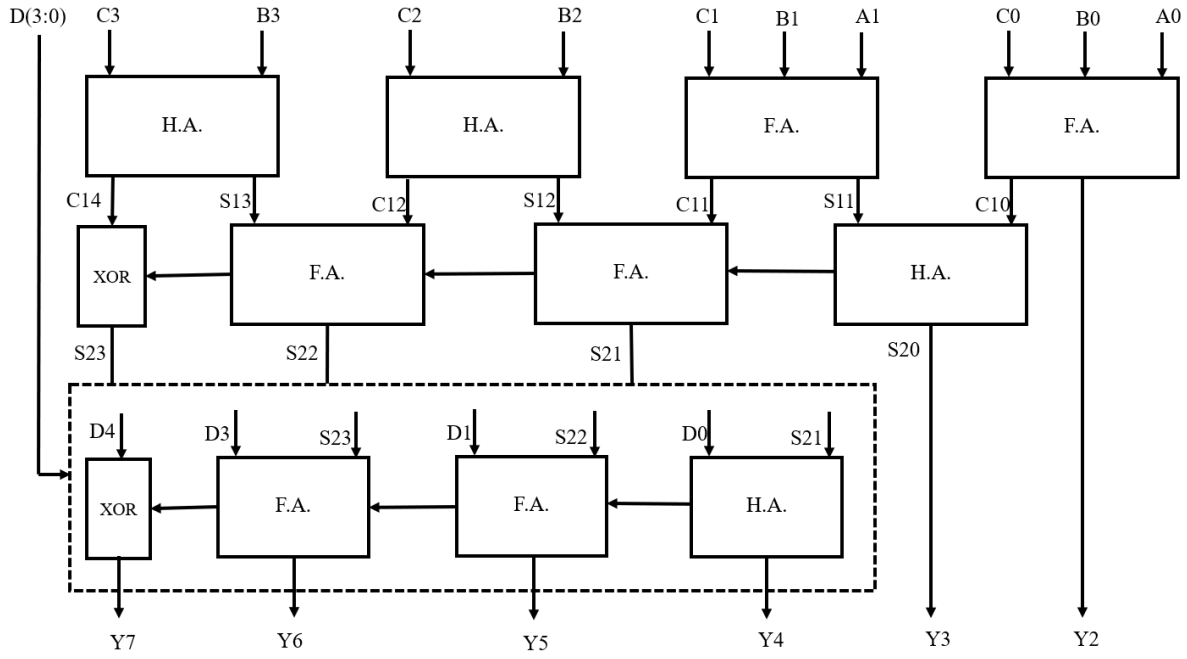



Fig. 6: Customized Hybrid Adder (CHA) block diagram

Addition performed in 3 stages. The first and second stage combinedly performed as a CSA architecture. After then Fourth input and out of CSA perform addition like a Ripple Carry Adder and final output found.This CHA minimized delay, power, and hardware. After then CHA is used as a component in 4×4 MVD. It makes MVD design also hardware efficient. Because CHA is a major component of 4×4 MVD. In the same manner, we can develop a higher order of CHA and MVD.

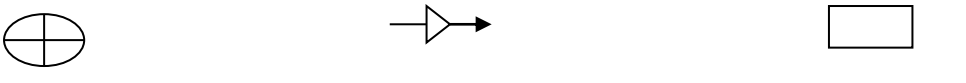
1.2.Ripple Carry Adder (RCA)

RCA is used in high-speed arithmetic operations of signal processing for optimizing area, power, and delay. It is used for high-speed operation, small area, and low power consumption instead of CSLA(RCA).This deliberation would also reduce the time delay [36].

4.3 Seamless Pipeline (SM)

The pipelining technique is used for delay minimization at the cost of the area. In 2016, P.K. Mehar produced the concept of a seamless pipeline [35]. By using this concept, it shows the importance of a seamless approach to the pipeline. It is based on the balancing of pipeline and it proved by using various examples it provides around 7 to11 % delay minimizations in various cases. In our proposed FIR filter design, it used seamless pipeline techniques of delay minimizations. The basic architecture of the FIR filter is shown in Figure 7.

The symbol used in the FIR filter structure



Adder Multiplier Delay element

Computations of equation (1) can be performed using the direct form-1 structure shown in Figure 7.

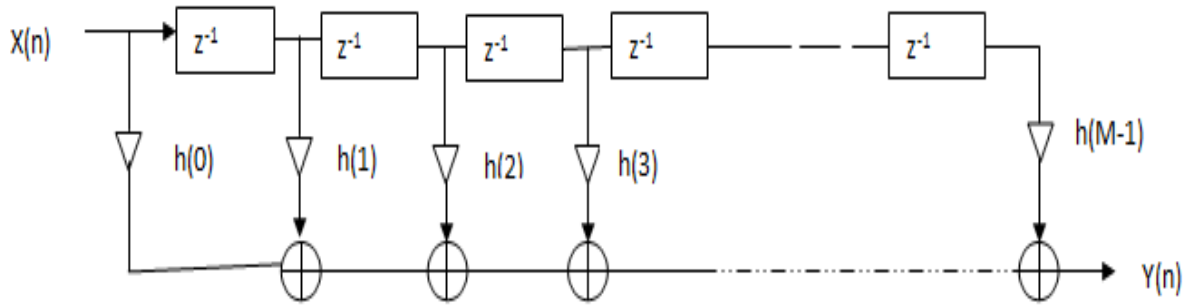



Fig.7. FIR direct -1 form structure

## III. RESULTS

Based on theoretical research and experimentation, we mainly addressed the results of the proposed method in this section. This section also describes measures of the efficiency of different well-known experimental parameters and settings. ASIC performance testing is carried out using an ASIC output. The test system used an i7, and 8 GB RAM processor and 225 SDD and 2 TB hard disc drives in the 8th generation. To enforce this architecture, the VHDL language is used. In the Xilinx 16.2 series, the VHDL code is implemented. ASIC performance testing package for the 2017 Cadence Genus package is used such as Field, Delay, Intensity, and Area Delay Product (ADP). ASIC hardware resources are tested by the 45 nm technology. The entire results section has been divided into two-part. In the first part, we discuss theoretical results and in the second part, we discuss Genus-based simulation results. Table 1 shown the theoretical hardware estimation of proposed 4-Bit and 8-Bit MVD and existing 4-Bit and 8-Bit Vedic multiplier design. Sumalatha et al. Vedic multipliers took 58 AND, 17 OR, and 42 XOR gate for 4-bit VD design implementation [27]. Padmavathy et al. took 53 AND, 8 OR, and 26 XOR gate for 4-bit VD design implementation [28]. Our proposed 4-bit MVD designs took only 40 AND, 6 OR, and 26 XOR gate for implementation. In the same manner, Sumalatha et al.

| | Bit Size | No. of Basic gate used for hardware implementations | | |
|---|---|---|---|---|
| | | AND | OR | XOR |
| Sumalatha et al. (2019) [27] | 4-Bit | 58 | 17 | 42 |
| | 8-Bit | 282 | 91 | 218 |
| Padmavathy et al. (2020) [28] | 4-Bit | 53 | 8 | 26 |
| | 8-Bit | 260 | 56 | 152 |
| Proposed MVD | 4-Bit | 40 | 6 | 26 |

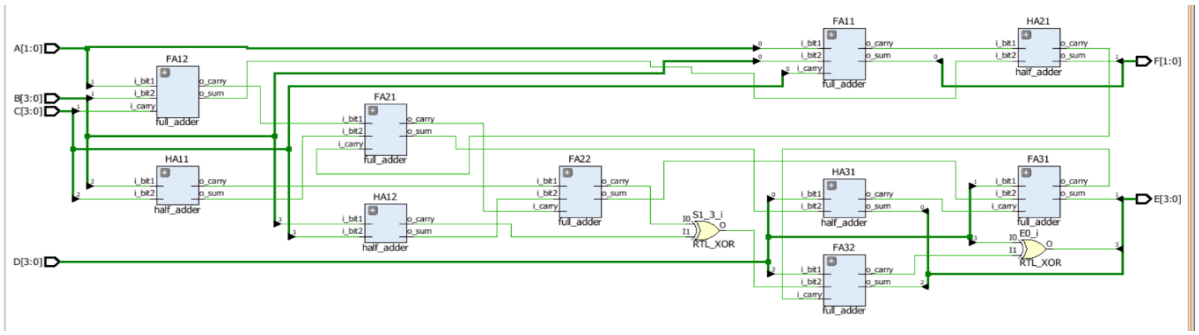
| | | | | |
|---|---|---|---|---|
| | 8-Bit | 196 | 38 | 142 |

Table 1. Theoretical hardware estimation of proposed 4-Bit and 8-Bit MVD and existing 4-Bit and 8-Bit Vedic multiplier design

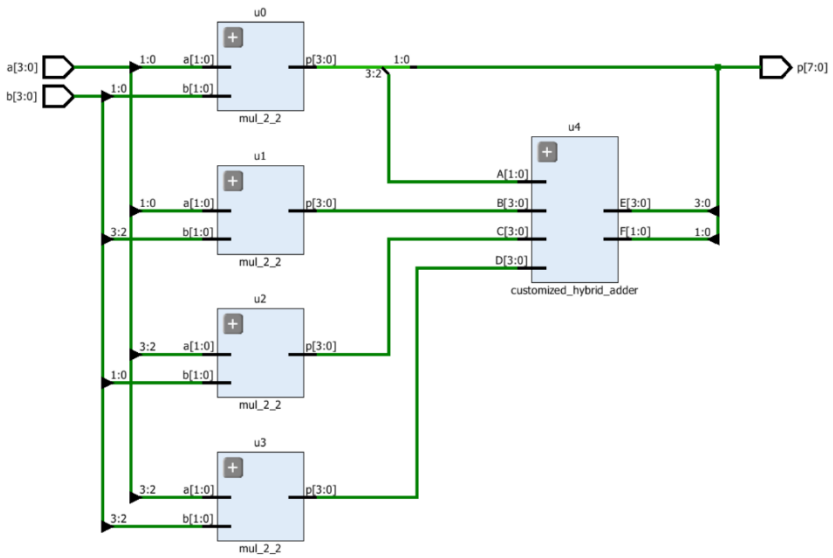
Vedic multipliers took 282 AND, 91 OR, and 218 XOR gate for 8-bit VD design implementation [27]. Padmavathy et al. took 260 AND, 56 OR, and 152 XOR gate for 8-bit VD design implementation [28]. Our proposed 8-Bit MVD designs took only 196 AND, 38 OR, and 42 XOR gate for implementation. Theoretical it has shown good margin in terms of area.

1.3.Simulation-based results

To enforce this architecture, the VHDL language is used. In the Xilinx 16.2 series, the VHDL code is implemented. RTL generated diagram of 4-Bit CHA is shown in Fig. 8. RTL generated diagram of 4-Bit MVD design is shown in Fig. 9.

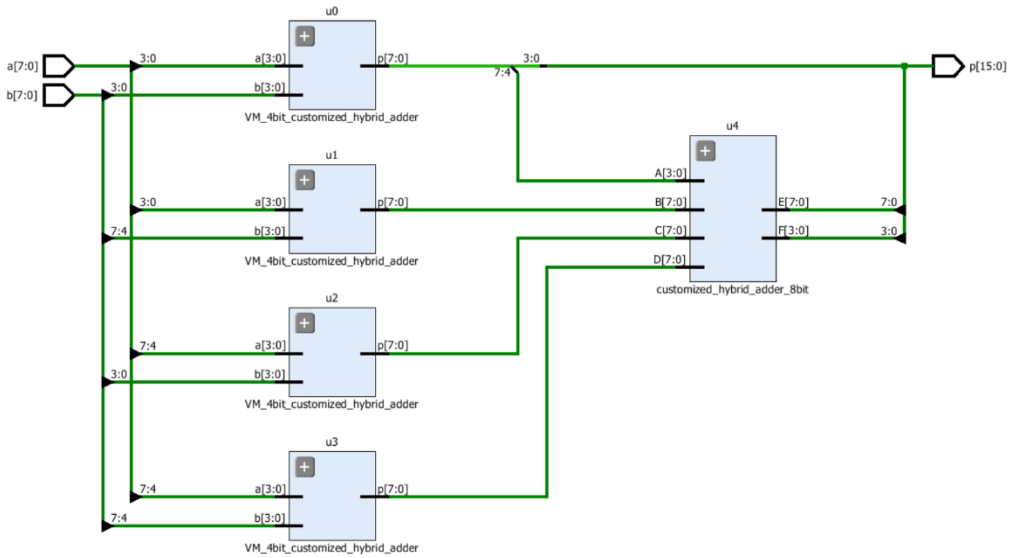



Fiq.8. RTL schematic diagram of 4-Bit CHA

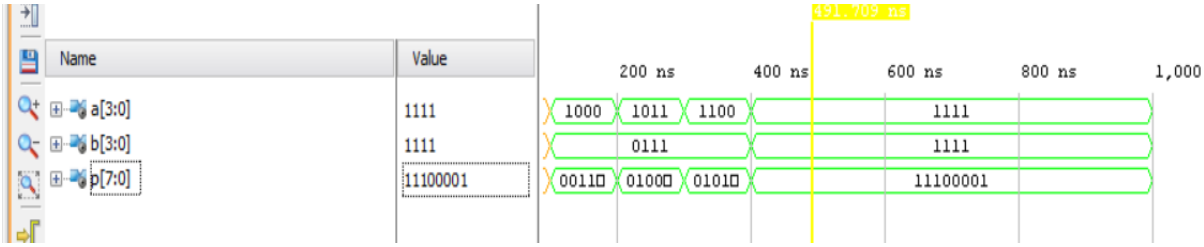



Fiq.9. RTL schematic diagram of 4-Bit MVD design

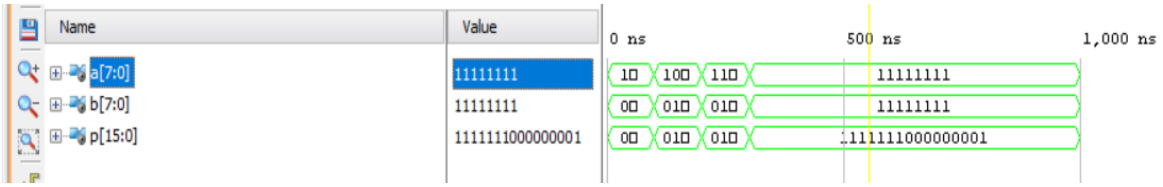
. RTL generated diagram of 8-Bit MVD design is shown in Fig. 10. The test bench generated for output verification for 4-Bit MVD design is shown in Fig. 11, and for 8-Bit MVD design is shown in Fig. 12.




Fiq.10. RTL schematic diagram of 8-Bit MVD design




Fiq.11. Test bench for output verification for 4-Bit MVD design




Fiq.12. Test bench for output verification for 8-Bit MVD design

ASIC performance testing package for the 2017 Cadence Genus package is used such as Area, Delay, Power, and Area Delay Product (ADP). ASIC hardware resources are tested by the 45 nm technology. Here, we simulated our proposed MVD design and existing VD also and achieved results are shown in Table 2. We simulated both designs for 4-Bit, 8-Bit, and 16-Bit. Padmavathy et al. took 192 $um^2$area, 547 PS delay, 6520.443 nW Power, 105024 $um^2$∗nW ADP and 1251925 $um^2$∗nWAPP for 4-bit VD design implementation [28]. Our proposed 4-bit MVD designs took only 158 $um^2$area, 480 PS delay, 4754.517nW Power, 75840$um^2$∗nW ADP and 751213$um^2$∗nW APP for implementation.

| | Bit size | Area ($um^2$) | Delay (PS) | Power (nW) | ADP ($um^2*nW$) | APP ($um^2*nW$) |
|---|---|---|---|---|---|---|
| Padmavathy et al. (2020) [28] | 4-Bit | 192 | 547 | 6520.443 | 105024 | 1251925 |
| | 8-Bit | 798 | 846 | 24712.584 | 675108 | 19720642 |
| | 16-Bit | 3706 | 1648 | 169704.249 | 6107488 | 629263355 |
| Proposed MVD | 4-Bit | 158 | 480 | 4754.517 | 75840 | 751213 |
| | 8-Bit | 514 | 733 | 17077.977 | 376762 | 8778080 |
| | 16-Bit | 2393 | 1119 | 83362.585 | 2677767 | 199486666 |

Table 2. Cadence Genus based hardware simulation results of proposed 4-Bit and 8-Bit MVD and existing 4-Bit and 8-Bit Vedic multiplier design

Padmavathy et al. took 798 $um^2$area, 846 PS delay, 24712.584nW Power, 675108$um^2*nW$ ADP and 19720642$um^2*nW$ APP for 8-bit VD design implementation [28]. Our proposed 8-bit MVD designs took only 514 $um^2$area, 733 PS delay, 17077.977nW Power, 376762$um^2*nW$ ADP and 8778080$um^2*nW$ APP for implementation.Padmavathy et al. took 3706 $um^2$area, 1648 PS delay, 169704.249nW Power, 6107488$um^2*nW$ ADP and 629263355$um^2*nW$ APP for 16-bit VD design implementation [28]. Our proposed 4-bit MVD designs took only 2393 $um^2$area, 1119 PS delay, 83362.585nW Power, 2677767$um^2*nW$ ADP and 199486666$um^2*nW$ APP for implementation. Our proposed design shows much decent gain in terms of area, delay, power, ADP, and APP.

By using the same MVD design with library Xilinx 16.2 inbuilt adder circuit, we developed an 8-Bit input 16 TAP FIR filter and existing design multiplier with library Xilinx 16.2 inbuilt adder circuit. Generated results are shown in Table 3. We found Padmavathy et al. took 14971 $um^2$area, 1290 PS delay, 639876.387nW Power, 19312590$um^2*nW$ ADP and 9579589390$um^2*nW$ APP for 16-bit VD design implementation [28]. Our proposed 8-Bit input 16 TAP FIR filter designs took only 10434 $um^2$area, 1317 PS delay, 766671.718nW Power, 13741578$um^2*nW$ ADP and 7999452710$um^2*nW$ APP for implementation.

| | Bit size | Area | Delay (PS) | Power (nW) | ADP ($um^2*nW$) | APP ($um^2*nW$) |
|---|---|---|---|---|---|---|
| Padmavathy et al. (2020) [28] | 16-Bit | 14971 | 1290 | 639876.387 | 19312590 | 9579589390 |
| MVD-FIR Filter | 16-Bit | 10434 | 1317 | 766671.718 | 13741578 | 7999452710 |

Table 3. Cadence Genus based hardware simulation results of proposed 8-Bit 16 TAP MVD FIR Filter and existing 8-Bit 16 TAP FIR Filter design

We simulate our design MVD-RCA-SP-FIR Filter design for 4-Bit, 8-Bit, and 16-Bit and existing results export from reference 28. Simulated results for MVD-RCA-SP-FIR Filter design for 4-Bit, 8-Bit, and 16-Bit and existing results are shown in Table 4.

| | Bit size | Area | Delay (PS) | Power (nW) | ADP($um^2*nW$) | APP ($um^2*nW$) |
|---|---|---|---|---|---|---|
| Padmavathy et | 8-Bit | 9845 | 2612 | 1111,720 | 28,355,486 | 12,234,900,101 |

| | | | | | | |
|---|---|---|---|---|---|---|
| al. (2020) [28] | 16-Bit | 30,102 | 2099 | 1311,234 | 69,771,012 | 48,232,148,120 |
| Proposed MVD-RCA-SP FIR Filter | 4-Bit | 3638 | 1387 | 162310.982 | 5045906 | 590487418 |
| | 8-Bit | 9321 | 1706 | 433466.745 | 15901626 | 4040343530 |
| | 16-Bit | 15178 | 1657 | 789563.986 | 25149946 | 11984002392 |

Table 4. Cadence Genus based hardware simulation results of proposed MVD FIR Filter and existing FIR Filter design

Results from Tables 1, 2, 3, and 4 clearly shown that objective of this work to developed an optimized design of MVD and FIR filter for ECG denoising is full fill.

## IV. CONCLUSION

In this paper, an FIR philter with modified Vedic multiplier-based architecture is introduced to carry out an ECG denoising application. This paper presents the first resource-efficient Vedic multiplier, which is approximately 55 percent area-efficient for 8 bit, 15 percent delay-efficient, and 45 percent power-efficient compared to the latest version proposed in 2020. Then the modified Vedic multiplier FIR is built, which is also efficient in terms of resources. It has a great ADP of 40.5 percent and a better APP of about 20 percent. This new philter design is very helpful for ECG signal denoising.With the proposed method, it is evident that the objective of this work to developed an optimized design of MVD and FIR filter for ECG denoising is full fill.

## V. REFERENCE

1. T.G. Keshavamurthy and M. N. Eshwarappa, "Review paper on denoising of ECG signal," *2017 Second International Conference on Electrical, Computer and Communication Technologies (ICECCT)*, Coimbatore, 2017, pp. 1-4, doi: 10.1109/ICECCT.2017.8117941.
2. C. Lastre-Domínguez, Y. S. Shmaliy, O. Ibarra-Manzano and M. Vazquez-Olguin, "Denoising and Features Extraction of ECG Signals in State Space Using Unbiased FIR Smoothing," in *IEEE Access*, vol. 7, pp. 152166-152178, 2019, doi: 10.1109/ACCESS.2019.2948067.
3. C. Brser et al., “Ambient and unobtrusive cardiorespiratory monitoring techniques,” IEEE Reviews Biomed. Eng., vol. 8, pp. 30-43, 2015.
4. M. Forouzanfar et al., “Oscillometric blood pressure estimation: past, present, and future,” IEEE Reviews Biomed. Eng., vol. 8, pp. 44-63, 2015.
5. J. S. Arteaga-Falconi, H. Al Osman, and A. El Saddik, “ECG authentication for mobile devices,” IEEE Trans. Instrum. Meas., vol. 65, no. 3, Mar. 2016.
6. S. Kiranyaz, T. Ince, and M. Gabbouj, “Real-Time patient-specific ECG classification by 1-D convolutional neural networks,” IEEE Trans. Biomed. Eng., vol. 63, no. 3, pp. 664-675, March 2016.
7. C. Ye, B. Kumar, and M. Coimbra, “An automatic subject-adaptable heartbeat classifier based on multi-view learning,” IEEE J. Biomed. Health Informatics, vol. 20, No. 06, pp. 1485-1492, Nov. 2016.
8. U. Satija, B. Ramkumar, and M. S. Manikandan, “Real-Time signal quality-aware ECG telemetry system for IoT-based health care monitoring,” IEEE Internet of Things Journal, Feb. 2017.

9. M. M. Sadaphule, S. B. Mule and S. O. Rajankar, "ECG Analysis Using Wavelet Transform and Neural Network," International Journal of Engineering Inventions, vol. 1, pp. 01-07, Dec. 2012.
10. S. Das, S. Mukherjee, S. Chatterjee and H. K. Chatterjee, "Noise elimination and ECG R peak detection using wavelet transform," *2016 IEEE 7th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON)*, New York, NY, 2016, pp. 1-5, doi: 10.1109/UEMCON.2016.7777876.
11. U. Satija, B. Ramkumar and M. S. Manikandan, "A Review of Signal Processing Techniques for Electrocardiogram Signal Quality Assessment," in *IEEE Reviews in Biomedical Engineering*, vol. 11, pp. 36-52, 2018, doi: 10.1109/RBME.2018.2810957.
12. C. Venkatesan, P. Karthigaikumar, A. Paul, S. Satheeskumaran and R. Kumar, "ECG Signal Preprocessing and SVM Classifier-Based Abnormality Detection in Remote Healthcare Applications," in *IEEE Access*, vol. 6, pp. 9767-9773, 2018, doi: 10.1109/ACCESS.2018.2794346.
13. J. Rodrigues, D. Belo, and H. Gamboa, ''Noise detection on ECG based on agglomerative clustering of morphological features,'' Comput. Biol. Med., vol. 87, pp. 322–334, Aug. 2017. doi: 10.1016/j.compbiomed.2017.06.009
14. H. Magsi, A. H. Sodhro, F. A. Chachar and S. A. K. Abro, "Analysis of signal noise reduction by using filters," *2018 International Conference on Computing, Mathematics and Engineering Technologies (iCoMET)*, Sukkur, 2018, pp. 1-6, doi: 10.1109/ICOMET.2018.8346412.
15. H. Gholam-Hosseini, H. Nazeran and K. J. Reynolds, "ECG noise cancellation using digital filters," *Proceedings of the 2nd International Conference on Bioelectromagnetism (Cat. No.98TH8269)*, Melbourne, Victoria, Australia, 1998, pp. 151-152, doi: 10.1109/ICBEM.1998.666440.
16. Rahul Kher, "Signal processing techniques for removing noise from ECG signals", *J. Biomed. Eng. Res* 3 (2019): 1-9.
17. Jayant, Ankit, Tripti Singh, and Manpreet Kaur. "Different techniques to remove baseline wander from ECG signal." *International Journal of Emerging Research in Management and Technology* 2, no. 6 (2013): 16-9.
18. Leif Sornmo and Pablo Laguna. (2005) Bioelectric Signal Processing in Cardiac and Neurological Processing. 1st Ed., Elsevier Academic Press, ISBN: 9780124375529.
19. Tsao, Yu-Chi, and Ken Choi. "Area-efficient VLSI implementation for parallel linear-phase FIR digital filters of odd length based on fast FIR algorithm." *IEEE Transactions on Circuits and Systems II: Express Briefs* 59, no. 6 (2012): 371-375.
20. Park, Sang Yoon, and Pramod Kumar Meher. "Low-power, high-throughput, and low-area adaptive FIR filter based on distributed arithmetic." *IEEE Transactions on Circuits and Systems II: Express Briefs* 60, no. 6 (2013): 346-350.
21. Kumm, Martin, Konrad Möller, and Peter Zipf. "Reconfigurable FIR filter using distributed arithmetic on FPGAs." In *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2058-2061. IEEE, 2013.
22. Park, Sang Yoon, and Pramod Kumar Meher. "Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter." *IEEE Transactions on Circuits and Systems II: Express Briefs* 61, no. 7 (2014): 511-515.
23. Ramandeep Kaur, Rahul Malhotra, Sujay Deb, "MAC based FIR filter: A novel approach for low-power real-time de-noising of ECG signals", *VLSI Design and Test (VDAT) 2015 19th International Symposium on*, pp. 1-5, 2015.

24. Chen, Jiajia, Jinghong Tan, Chip-Hong Chang, and Feng Feng. "A new cost-aware sensitivity-driven algorithm for the design of FIR filters." *IEEE Transactions on Circuits and Systems I: Regular Papers* 64, no. 6 (2017): 1588-1598.
25. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan, "An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition," Elsevier, The integration, VLSI journal, Vol. 58, pp. 134-141, June 2017.
26. Madugula Sumalatha, Panchala Venkata Naganjaneyulu, Kodati Satya Prasad, Low power and low area VLSI implementation of Radix- 8 Carry look ahead adder FIR filter for DSP applications, J. Adv. Res. Dyn. Control Syst. 10 (10-Special Issue) (2018) 70–82.
27. Madugula Sumalatha, Panchala Venkata Naganjaneyulu, Kodati Satya Prasad, 2019. Low power and low area VLSI implementation of vedic design FIR filter for ECG signal de-noising. *Microprocessors and Microsystems*, *71*, p.102883.
28. Padmavathy, T.V., Saravanan, S. and Vimalkumar, M.N., 2020. Partial product addition in Vedic design-ripple carry adder design fir filter architecture for electro cardiogram (ECG) signal de-noising application. *Microprocessors and Microsystems*, p.103-113.
29. R. Rohini, N. V. Satya Narayana and Durgesh Nandan "A crystal view on design of FIR filter" Journal of Computational and Theoretical Nanoscience, Vol. 17, No. 7, 2020.
30. Durgesh Nandan, Jitendra Kanungo and Anurag Mahajan, "An errorless Gaussian filter for image processing by using expanded operand decomposition logarithm multiplication," Springer, Journal of ambient intelligence and humanized computing, 2018, DOI:10.1007/s12652-018-0933-x.
31. Durgesh Nandan, Mahajan, A. and Kanungo, J., "An efficient architecture of Iterative Logarithmic Multiplier," International journal of engineering & technology (UAE). Vol.7 (2.16), pp. 24-28, 2018.
32. E. Jagadeeswara Rao, Durgesh Nandan, R.V. Vijaya Krishna and K. Jayaram Kumar, "A Systematic Review of Multipliers: Accuracy and Performance Analysis," International Journal of Engineering and Advanced Technology (IJEAT), Volume-8 Issue-6S, pp. 965-969, August 2019.
33. S. R. Huddar, S. R. Rupanagudi, M. Kalpana and S. Mohan, "Novel high speed vedic mathematics multiplier using compressors," *2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s)*, Kottayam, 2013, pp. 465-469.
34. Jagadguru Swami S. Bharati KrisnaTirthaji maharaja,(1965) Vedic Mathematics or Sixteen Simple Mathematics formulae from the veda.
35. Meher, P.K. Seamless Pipelining of DSP Circuits. *Circuits Syst Signal Process* **35,** 1147–1162 (2016). https://doi.org/10.1007/s00034-015-0089-2
36. Sumalatha M., Naganjaneyulu P.V., Satya Prasad K. (2018) Low-Power and Area-Efficient FIR Filter Implementation Using CSLA with BEC. In: Anguera J., Satapathy S., Bhateja V., Sunitha K. (eds) Microelectronics, Electromagnetics and Telecommunications. Lecture Notes in Electrical Engineering, vol 471. Pp. 137-142, Springer, Singapore. https://doi.org/10.1007/978-981-10-7329-8_14