European Journal of Molecular & Clinical Medicine
ISSN 2515-8260 Volume 07, Issue 06, 2020

Fastest Multiplier Implementation Using Ancient Scriptures Algorithms: Review

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Abstract

In any of the fastest ALU, multiplier play an inevitable role. There is always a demand on high speed multiplier due to the raising limitation on delay. Increasing the speed of a multiplier there are number of new techniques have been implemented in which multiplier using Vedic mathematics are foremost one. Vedic mathematics are derived from ancient Vedas, it is mainly divided in to 16 sutras and upasutra in which Urdhva Thiryagbhayam and Nikhilam sutra are used for multiplication. Multiplier are used in different area such as cryptography, image processing application, embedded system application, programmable filter application etc. The multiplier efficiency are depended on their speed, delay and area .In this article different multiplier are compared with their efficiency and concluded that Vedic multiplier are most prominent along them.

Keywords: Urdhva Thiryagbhayam, Nikhilam sutra, Delay, Area, Multiplier

1 INTRODUCTION

Indian system of mathematics played a major role in ancient sculptures. **Jagadguru Shri Bharathi Krishna Tirthaji** was the person who rediscovered the Vedic system of mathematics in beginning of 20th century. Conventional mathematics contain more complex and tedious process for problem solving, it can reduce by using Vedic mathematics. Vedic mathematics are incorporated with 16 sutras and 13 upasutra. Vedic mathematics can apply to any area of mathematics example Integral, differential, geometry, trigonometry, addition, multiplication, division, root of the equation etc. Era of digitalization make high challenge on high speed digital circuit. High speed can achieved only through the high speed processor. Any of the processor speed can depend on the multiplier used on it.Multiplier is an essential part for any computation process. Conventional multiplier (Booth, Array, and Wallace Tree) can provide less efficiency in area, speed and power .For improving the efficiency of the multiplier, it can design using Vedic algorithm. Vedic algorithm can include less number of steps for multiplication so that efficiency of the system can increase. In this paper we make a survey on high speed Vedic multiplier.

2. Related Work

V.S Kumar Chunduri et al. [1] proposed an 8bit Vedic multiplier using Urdhva Tiryagbhyam algorithm in which analysis can be done using Xilinx hardware tool. This paper shows that the 8 bit Vedic multiplier has low power 82nW and high speed 145.03MHz as compared to conventional multiplier. The proposed multiplier shows high performance on higher order bit.
G. Ganesh Kumar et al.[2] implemented a 32x32 bit multiplier using Vedic algorithm .32 bit multiplier can produce a delay of 31. 52ns compare to conventional multiplier it concluded that Urdhva Tiryagbhyam, Nikhilam and Anurupye sutras are reduce the delay, power, and hardware requirements of multiplier compare to conventional multiplier.

Nishant.G.et al. [3] offering a 32x32 bit Vedic multiplier. In this paper multiplier attain a smaller delay of 6.46ns by using UT algorithm. For future work an integrated Vedic ALU is proposed for this article. And it concluded that Vedic multiplier are more efficient in terms of speed compare to other multiplier.

Ramanchandran.S et al. [4] designed an integrated Vedic multiplier architecture, in which multiplier architecture itself select the proper multiplication sutra. This will done through the applied input .If input is larger number of bit design selected the faster algorithm of Nikhilam Sutra, if input is smaller number of bit it selected the Urdhva Tiryagbhyam.

Surabhi Bhardwaj et al. [5] discovered an advance Vedic multiplier. In which basic multiplication can done using Urdhva Tiryagbhyam algorithm and accumulation process can done using Carry Select Adder. Compared to other16 bit multiplier proposed multiplier shows less delay of 30.659ns.

Beechu Naresh [6] designed a new multiplier especially for squaring application. It outcomes concluded that, this architecture is worth for high performance processor.

Prasanth D.Pawel et al. [7] gave implementation of new Vedic multiplier using UT algorithm and CLA adder addition method. In which it seen as high efficiency in speed and area compared to existing method.

Hemangi P. Patil et al. [8] proposed a new multiplier using Vedic algorithm and reversible logic. It showed that Nikhilam sutra using reversible gates can provide a high efficiency in terms of power, area and delay compared to conventional Vedic multiplier and Booth multiplier

S. Arish et.al [9] find out that combination of Karatsuba algorithm and Urdhva Tiryagbhyam algorithm of a multiplier shows percentage of reduction in area and delay when number of bit length is increased.

Valentina Bianchi et.al [10] proposed a new modular architecture of Vedic multiplier using 4:2 compressors instead of normal adders. It shows better solutions in terms of propagation delay and area.

Praveen Kumar Y G et al [11] make a study on different multipliers papers and he concluded that multiplier using UT Vedic algorithm is more prominent among power and speed compare to conventional multipliers.

No:	Title of the Paper	Publisher/ year	Algorithm or Method	Inference	Tool used	Efficiency based on power,delay,speed
1	Design and implementation of multiplier using KCM and vedic mathematics by using reversible adder	IJMER 2013	Urdhva Tiryagbhyam with reversible adder	Vedic Multiplier using reversible adder can provide a better performance in higher order multiplication	Modelsim and Xilinx spartan3E,FPGA kit	Area=180 Speed= 145.03MHz Power=82 mW (8x8 bit)
2	Design of high speed Vedic multiplier using Vedic mathematics techniques	IJSRP 2012	Urdhva Tiryagbhyam algorithm	Multiplier using UT algorithm provide minimum delay for multiplication in any type of input bit.	Xilinx Spartan XC3S500-5-FG320	Delay=31.526ns (32x32 bit)
3	Ancient Indian Vedic Mathematics based 32-Bit Multiplier Design for High Speed and Low Power Processors	IJCA 2014	Urdhva Tiryagbhyam algorithm	Complexity of the hardware can reduced for higher order input bit by using vedic multiplier	Modelsim Xilinx Virtex5 (XC5VLX110T	Delay=6.465ns (32x32 bit)

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4	Design implementation and performance analysis of an integrated vedic multiplier architecture	IJCER 2012	Urdhva Tiryagbhyam and Nikhilam sutra	Here conclude that for higher order bit multiplication Nikhilam sutra is favourable, on other hand lower bit multiplication UT algorithm is better	Xilinx ISE 11	Speed 32.816ns for 64bit 13.455ns for 8bit
5	Design of High Speed Multiplier using Vedic Mathematics.	IJERGS 2014	UT algorithm for multiplication and Carry Save Adder for accumulation	UT algorithm with CSA provide less delay compared to conventional type multiplier	Modelsim Xilinx Spartan 3 Xc3s50-4	Delay= 30.659ns (16x16 bit)
6	Design and implementation of high performance and area efficient square architecture using Vedic Mathematics	Analog integrated circuit and signal processing 2019	Anurupye Sutra	Compared to the Existing squaring circuit proposed architecture is most useful for high performance processor.	Vivado design suite 2018.3k intex-7 FPGA	Delay= 38.6ns (64x64 bit)
7	High speed Vedic multiplier design and implementation on FPGA	IJAR 2015	UT algorithm with compressor and CLA adder	For 16 bit multiplication 7:3 compressor are used and also it show high benefits on speed and area, but number of transistor used is high.	Xilinx XC3s200-4tq.144	Area are represented by number of LUT used 679.
8	FPGA implementation of conventional and vedic algorithm for energy efficient multiplier	IEEE 2015	Nikhilam sutra with reversible logic	Using reversible logic in vedic multiplier can reduced the power dissipation and make the system more efficient.	Xilinx Spartan 3E 3s250e VQ-100 FPGA	Delay= 8.73ns Power= 82mW.
9	Run-Time-Reconfigurable Multi-Precision Floating-Point Matrix Multiplier Intellectual Property Core on FPGA	Circuit system and signal proce	Karatsuba algorithm and Urdhva Tiryagbhyam algorithm	Percentage reduction in area, power and delay when number of bit length of multiplier is increased.	Xilinx ISE 14.7 Virtex 5 ML10	Delay= 11.514ns (16x16 bit)

		ssing 2017				
10	A modular Vedic multiplier architecture for model-based design and deployment on FPGA platforms	Micr opro cesso rs and Micr osyst ems 2020	Urdhva Tiryagbhyam algorithm With 4:2 compressor	This design shows a better performance in area and delay compare to Wallace tree, Booth and 4:2 compressor reference multipliers.	Xilinx VIVAD O Artix 7 FPGA.	Number of LUT used in 32 bit multiplier =1086

Table 1: survey of high speed multiplier using Vedic mathematics techniques

3 CONCLUSION

In this survey we focused on the various type of Vedic multiplier and it shows a high efficiency in speed, delay and power compare to conventional multipliers. These multipliers have a large application in many areas such as Dsp, Fft, Filters, Biomedical application, image processing and also in cryptography.

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