European Journal of Molecular & Clinical Medicine
ISSN 2515-8260 Volume 07, Issue 9, 2020

Analyzing Performance and Pulse Width Modulation Control and Digital Control Approach for Asymmetric DC-AC Cascaded H Bridge Multilevel Inverter

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Abstract
There have been many pieces of research done that showcase the limitations of high power output and voltage in conventional inverters. Multilevel inverters are among the most used form of inverter today simply because of their efficiency, enhanced power ratings and harmonic profiles. The following article consists of a detailed evaluation of the power, pulse width analysis, and the digital control mechanisms and approaches for a 5 level cascaded H-Bridge multilevel inverter. The analysis of the CHMI or cascaded H-bridge multilevel inverter has been done by Simulink and MATLAB software. Total harmonic distortion, harmonic spectrum, waveform patterns and output voltage has been chosen as the analysis parameters here. Apart from all these analysis discussion and evaluation regarding the control schemes has also been presented in the article.

Introduction

Power electronic applications that require AC output frequency and magnitude have been using Switch-mode inverters. Both three-phase and single-phase AC systems have been using inverters. As per Usha et al. (2018), one of the simplest forms of inverters is the half-bridge inverters as they are able to produce square-wave waveform outputs. Such inverters usually require a centre-tapped voltage source supply. Contrarily, two-level and three-level output waveforms require full-bridge topologies.

Though famously used for a wide variety of electronic appliances, there are many drawbacks to such forms of inverters in the aspects of high power conversion and voltage. Transformers are used to reduce harmonic distortion and increasing the voltage capacity of these inverters. This reduces the factors of high cost, bulkiness and voltage loss of the AC systems. Other than that, there are disadvantages related to the high-frequency operation of these inverters because of device constraints ratings and switching losses (Peddapelli 2016).

Due to all these factors, multilevel inverters have been developed, and are becoming infamous due to the advantages they provide regarding harmonics reduction and high voltage creation. A number of industrial power applications use multilevel inverters for operations regarding drive systems, static VAR compensators and AC power supplies. The work by synthesizing the output AC terminal voltages from DC voltage sources, producing staircase output waveforms. Such a procedure allows lessening of the voltage stress of the switches and enhances the output voltage ratio.

Upon review of the facts and evidence regarding multilevel inverters, it was seen that they have been increasingly been famous for the last 24 years. Cascaded H-bridge multilevel inverters or the CHMI's are one of the simpler versions of multilevel inverters.

Cascaded H-Bridge multilevel Inverters

As the name suggests, this specific inverter produces inverted AC from the separate DC sources using the full potential of the H- bridges. Natural resources like wind energy, sunlight, etc. can be used as the DC sources for these inverters. Mahfuz-Ur-Rahman et al. (2016) stated that one of the potential advantages of these inverters is that they don't need any diodes or capacitors for clamping purposes. The output AC wave is mostly in the form of sine curves even without any form of filtration.

Configuration of a three-phase CHMI circuit

The configuration of a three-phase CHMI circuit system is nothing but a connection between three single-phase CHMI circuits (Siddique and Sarwar 2016). The configuration can be either of wye form or delta form. The circuit system requires eight switches per phase and two H=bridge cells. It means that overall 24 power switches and 6 H-bridge cells are required for the complete configuration. It also translates to the generation of 12 pairs of gating signals for the inclusive switches within the configuration. For each of the H-bridge cells, the inclusive switches are constructed in such a way that one pair operates the reference frequency while the other, carrier frequency. Such a switching system translates to two low-frequency switches as well as two high-frequency switches.

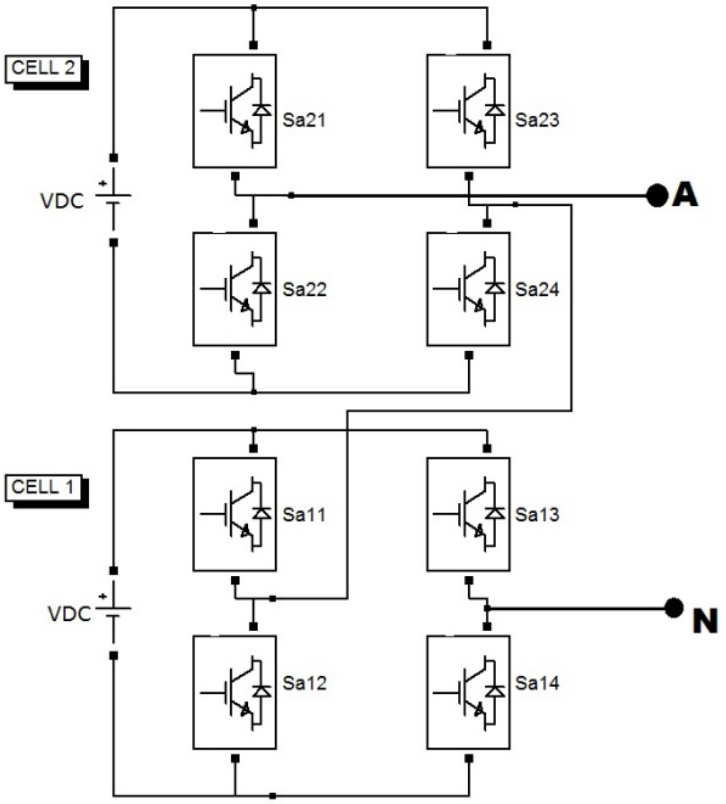

Figure 1: Circuit configuration of a three-phase 5 level cascaded H-bridge inverter
(Source: Akalya et al. 2017, p. 39)

In the figure provided above, V_{AN} is the summation of V_{a1}, V_{a2} ...$V_{a(S-1)}$ and V_{aS} and overall is the total voltage of phase A. Phase B and phase C also follows the same voltage distribution structure (Akalya et al. 2017). Now comes the line voltages. They can be computed using the formula mentioned below. For example, the line voltage between phase A and B is to be given a name then it will be named as V-AB. As per Shankar and Edward (2016), the computation formulae:

$V_{AB}= V_{AN}-V_{BN}$

The abbreviations are described as per their meaning below:

V_{BN} is the phase B voltage,

V_{AN} is the phase A voltage, and

V_{AB} is the line voltage between both the phases

Pulse width modulation technique

The method of the reduction of the average power delivered by an electric signal by dividing it into segmented parts can be described as a pulse-width modulation technique (Aly et al. 2017). The working procedure of the concerning technique is to use one modulation per phase along with several carrier signals. The bands that are occupied are always contiguous and the triangular

carriers of the respective inverter's amplitude and frequency are always disposed of. The signal produced by the modulation is often of a sine curve, or sinusoidal and reflects both the aspects of amplitude and frequency. During the modulation process, the signal produced is compared with the carrier signal at every instant. According to Moeini and Wang (2017), the core device remains off when there is no action in the comparison switches and is tuned on while the reference signal becomes higher than the assigned triangular carrier. The figure provided below showcased the pulse width modulation for a three-phase multilevel (5) cascaded H-bridge Inverter.

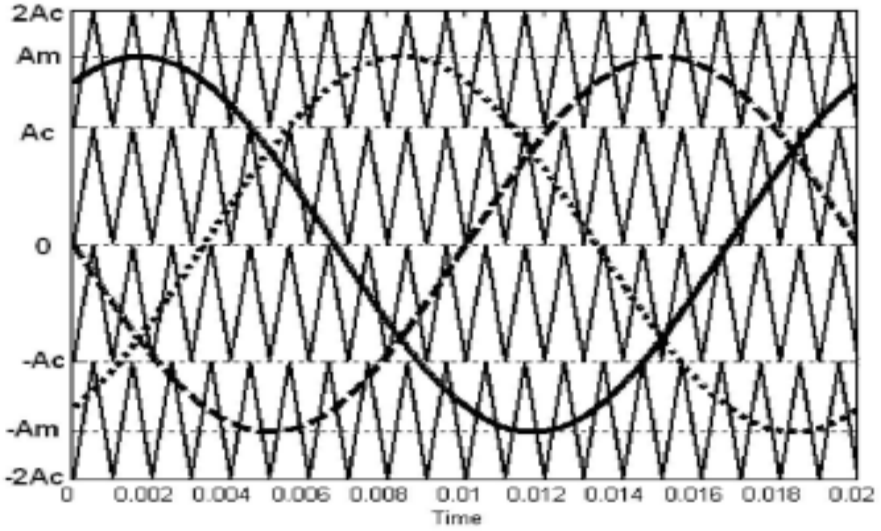

Figure 2: PWM waveform for a three-phase multilevel (5) cascaded H-bridge Inverter.

(Source: Moeini and Wang 2017, p. 7579)

The pulse width modulation technique or method is inclusive of three main parameters, one of which is referred to as frequency modulation index or m_f, which can be derived by:

$m_f = f_c/f_m$

The other parameter is inverter resistive load; which is usually described as:

$m_a = A_m/N' A_c$

The final parameter can be described as the displacement angle between the initial positive triangular carrier signals and the resulting modulating signal. During the pulse width modulation analysis process of this respective three-phase 5-level cascaded H-bridge inverter, the angle of displacement was found to be zero.

For the formulation of any PWM strategy, harmonic frequency or (*mx+py)* calculation evaluation is also of utmost importance. The mathematical formulas that assist in calculating the sinusoidal harmonic component of the time varying switched waveforms are expressed below:

$v(t) = \frac{a_0}{2} + \sum_{p=1}^{\infty}\{a_{0p}\cos py + b_{0p}\sin py\}$ (Baseband and fundamental harmonics)

$+ \sum_{m=1}^{\infty}\{a_{m0}\cos(mx+py) + b_{mp}\sin(mx+py)\}$ (Equation for calculating carrier harmonics)

$+\sum_{m=1}^{\infty}\sum_{p=-\infty}^{\infty}\{a_{mp}\cos(mx+py) + b_{mp}\sin(mx+py)\}$ (Where p ≠0) (Equation for formulating carrier sideband harmonics)

Digital control approach of CHMI power width modulation

Conventionally, there are three forms of techniques for formulating the power width modulation graph of a cascaded H- bridge multilevel inverter. As per Busarello et al. (2019), these techniques are known as PS or Phase Shifted technique, CD or Carrier Disposition technique and H or hybrid technique respectively. Usually, the carrier distribution method is the most popular form of power width modulation as the sampling of the reference waveforms is done by the contiguous increments of the reference waveform amplitudes and carrier waveform displacements. The phase-shifted method, on the other hand, uses the phase shifts of all the relevant carriers. The hybrid method, as the name suggests is the combination of both of these techniques. CD method popularly used for providing various schemes related to the same aspect. These schemes are respectively known as POD or Phase Opposition Disposition, APOD or Alternative Phase Opposition Disposition and lastly PD or Phase Disposition (Venkataramanaiah et al. 2017).

The power width distribution figure provided above also consists of zero phase reference value and POD scheme carrier signals. The displacement of the waveforms is noted to be 180° above the zero phase values, whereas the alternative phase opposition disposition scheme requires an alternate displacement of about 180° from its respective adjacent carriers. The analysis figures listed in this article has been produced using all the mentioned carrier disposition technique schemes, but the PD scheme analysis was given a bit more emphasis.

All the forms of power width modulation and simulation have been done using MATLAB/Simulink. They decided parameters for the formation of the simulations have been provided in the table below.

Parameter	**Value**
Fundamental Frequency	50 Hz
Resistance	100Ω
Inductance	318.5mH
Carrier frequency	5.2 kHz
Modulation Index	1
DC Bus Voltage	

The detected polarity of the sine waves of the power width modulation figures was found out to be unipolar in nature. The logic circuit and the comparator generate negative levels of voltage if the polarity of the sine waves is found out to be negative while contrarily, it generates a positive voltage when the logic circuit levels are positive. According to Kumar and Pal (2019), the ratio between the KA_C and the instantaneous reference wave values determine the final output voltage level value. It is further regulated by adjusting the value of M. The value of M is further adjusted by controlling the PI or the proportional plus integrals of the controller. This enables the controller to process any potential errors in the actual output voltage and the desired output voltage measures.

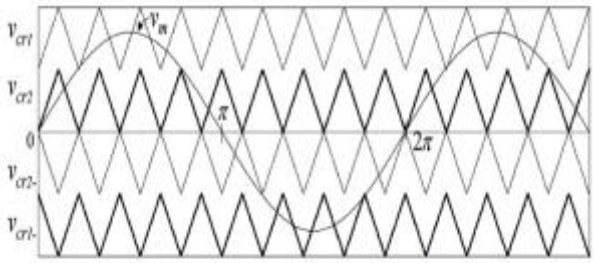

Figure.3 Carrier arrangement for POD

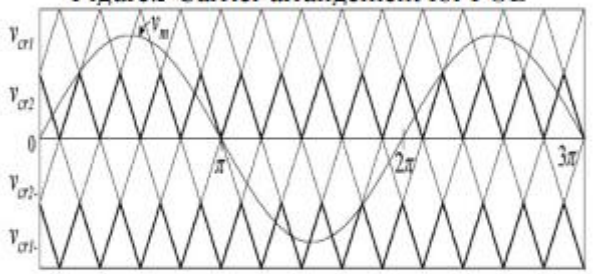

Figure.4 Carrier arrangement for APOD

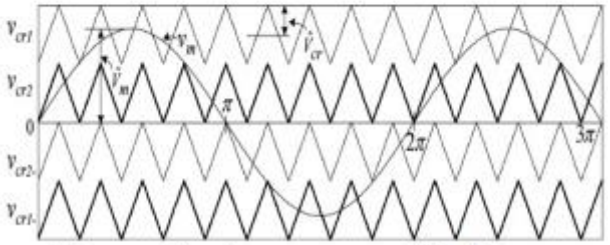

Figure.5 Carrier arrangement for PD

(Source: self-created by author)

The above figure showcases the carrier arrangement of the three-phase 5-level cascaded H-bridge inverter according to the parameters set in the MATLAB/Simulink software.

Figures have been provided below for showcasing the phase voltage, line voltage and load current waveforms output of three-phase 5-level cascaded H-bridge inverter that has been formulated through MATLAB Simulink Software.

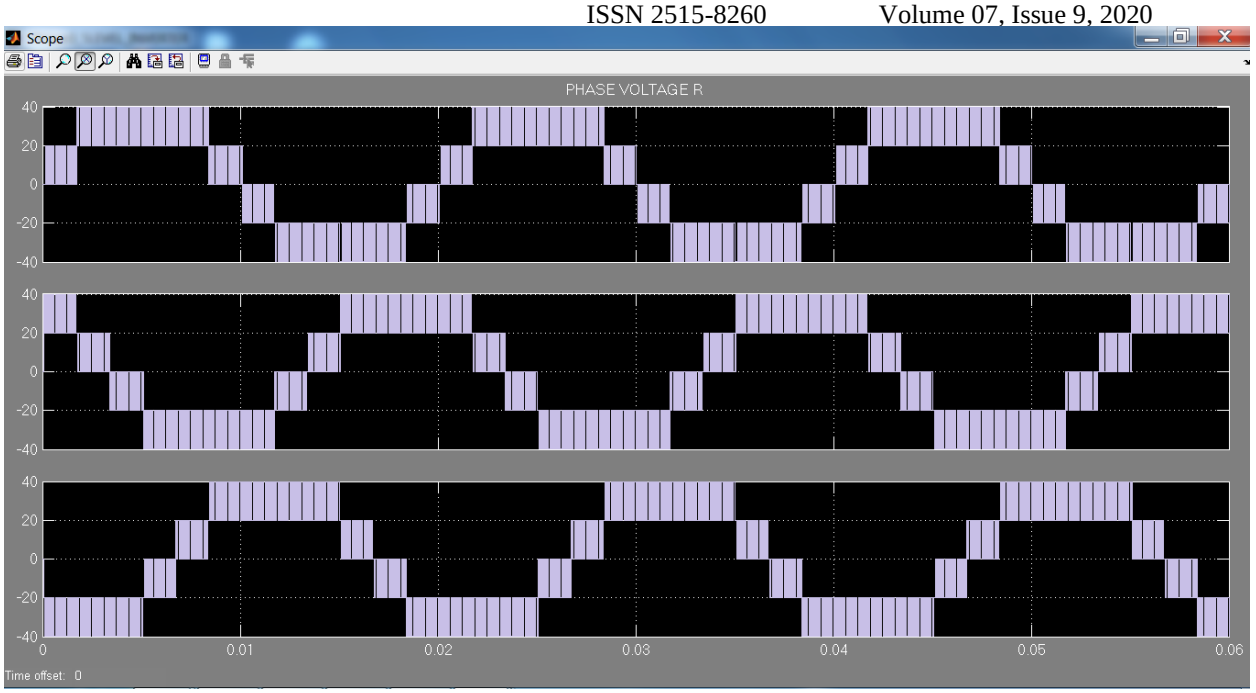

Figure 6: MATLAB Simulink graph for three-phase 5-level cascaded H-bridge inverter phase voltage output.

(Source: self-created by author)

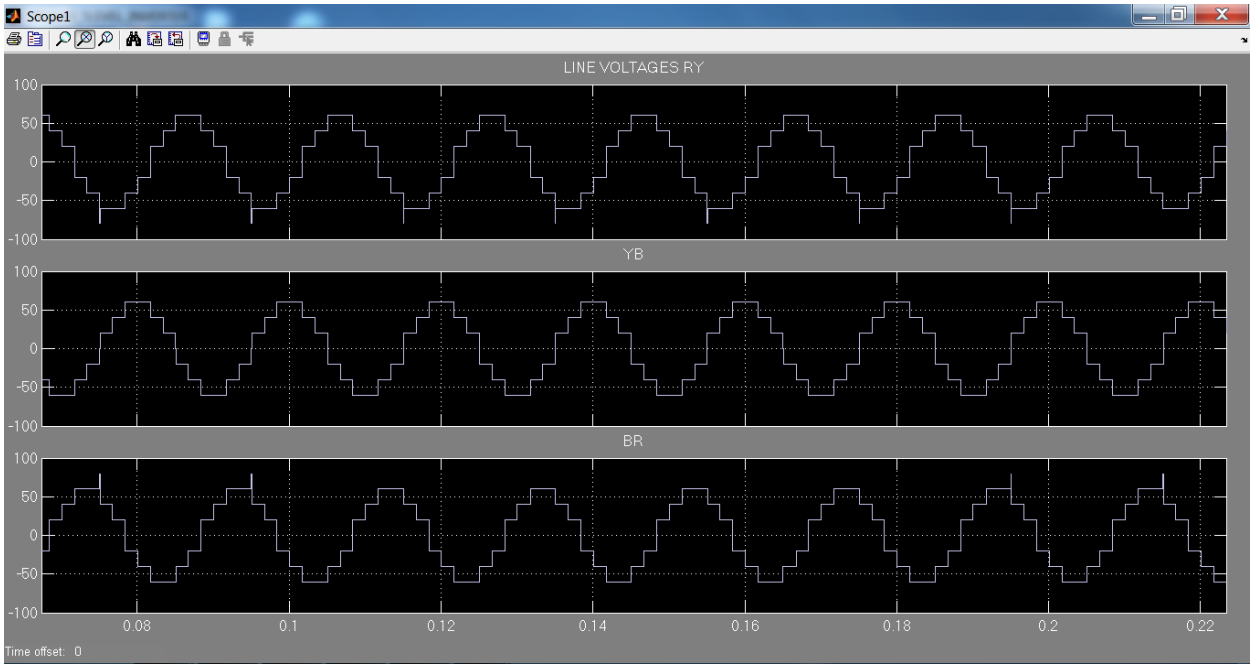

Figure 7: MATLAB Simulink graph for three-phase 5-level cascaded H-bridge inverter line voltage output.

(Source: self-created by author)

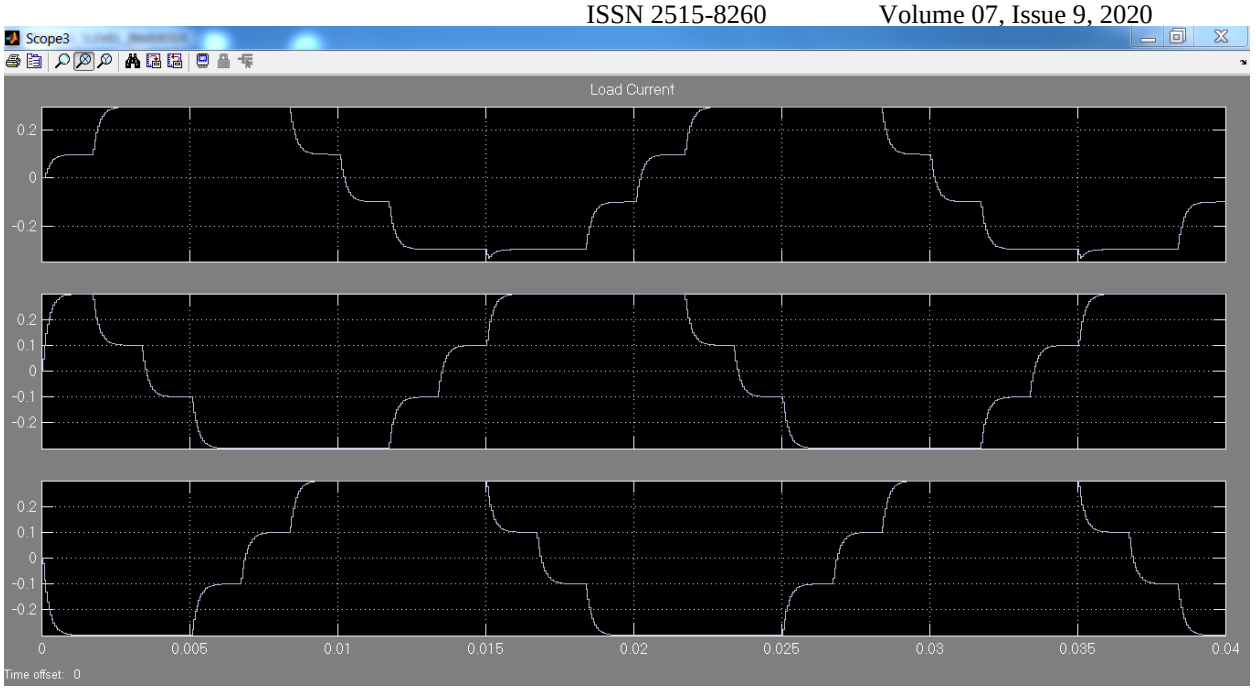

Figure 8: MATLAB Simulink graph for three-phase 5-level cascaded H-bridge inverter load current output.

(Source: self-created by author)

Inverter efficiency and power loss

One of the most important aspects of multilevel inverters is the cooling system designation and the cost estimation index. These aspects can also be related to the aspect of power loss of the inverter. Usually, multilevel inverters showcase two forms of semiconductor losses. The loss in conduction is usually experienced due to the drop in the voltage during the process of current conduction by the semiconductors. On the other hand, another form of loss, known as the switching loss is also experienced when the switching frequency gets fluctuated during the process of current commutation. As per Dhanamjayulu and Meikandasivam (2017), there are also other forms of losses experienced, namely, off-state losses and snubbers, but such losses occur on a very minute scale and hence are disregarded.

The figures provided below showcase the different forms of power losses experienced during the analysis process of the three-phase 5- level cascaded H-bridge asymmetrical inverter.

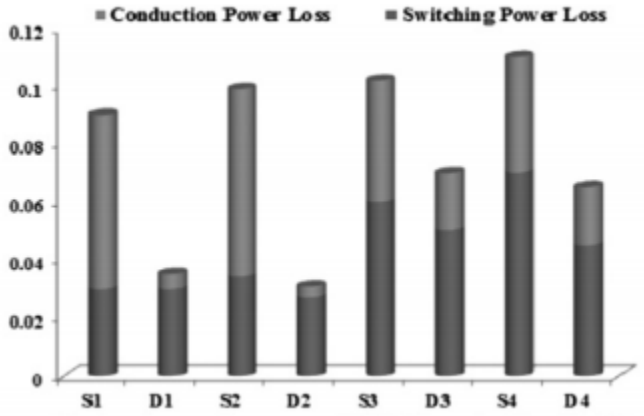

Figure 9: Switching and conduction power loss of three-phase 5- level cascaded H-bridge asymmetrical inverter

(Source: Dhanamjayulu and Meikandasivam 2017, p. 739)

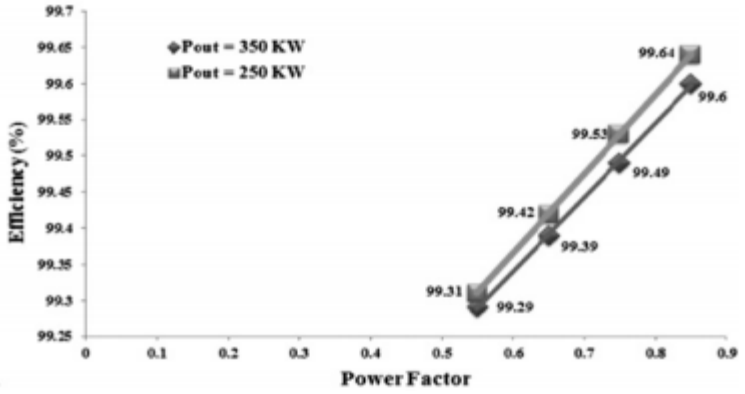

Figure 10: Power factor- efficiency ratio of three-phase 5- level cascaded H-bridge asymmetrical inverter

(Source: self-created by author)

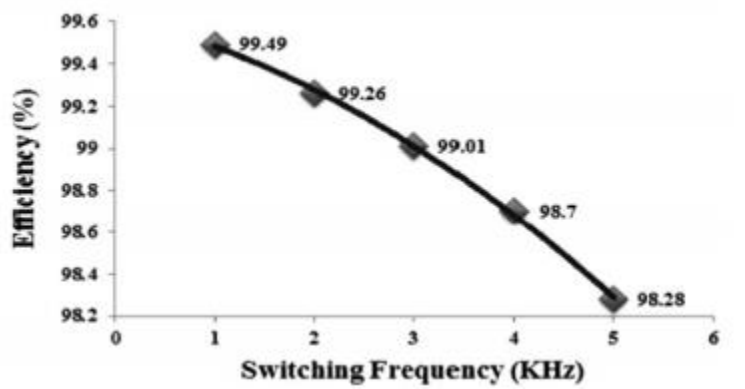

Figure 11: Switching Frequency-efficiency ratio of three-phase 5- level cascaded H-bridge asymmetrical inverter.

(Source: self-created by author)

Total harmonic Distortion

As per Jayabalan et al. (2017), one of the major aspects for voltage output comparison for any form of inverters is to measure the total harmonic distortion or the THD of the respective inverter model. Usually, the waveforms or curves incurred from the simulations showcase sinusoidal curves which are smooth and even. When any form of distortion occurs in the circuits, these smooth curves tend to be jagged lines, which can translate to various forms of efficiency issues. Usually, the aim for any form of electronic equipment and current suppliers is to lower the distortion ratios as much as possible (Busarello et al. 2017). The THD Graph of the three-phase 5-level cascaded H-bridge asymmetrical inverter has been provided below.

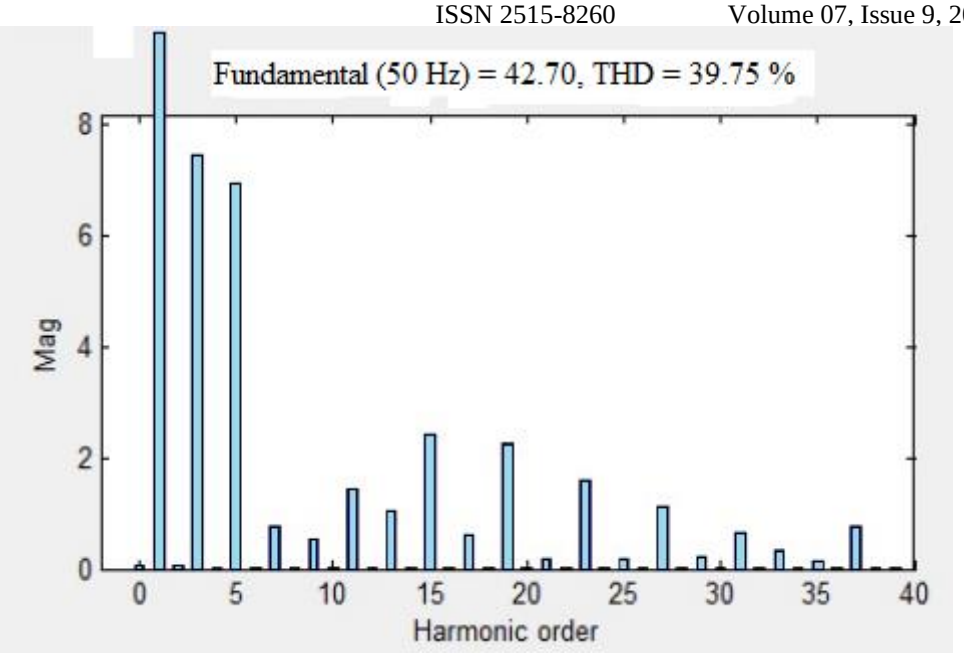

Figure 12: MATLAB Simulink formulated THD Graph for the three-phase 5- level cascaded H-bridge asymmetrical inverter.

(Source: self-created by author)

According to Kumar et al. (2019), during the analysis procedure that was conducted with the three-phase 5- level cascaded H-bridge asymmetrical inverter, it was found out that there was no additional benefit or reduction in the THD levels of the concerning inverter from those of the conventional multilevel inverters. But, the THD line voltage becomes the lowest when the high modulation strategy is introduced in the PD modulation strategy.

Conclusion

According to the analysis done regarding the three-phase 5- level cascaded H-bridge asymmetrical inverter, it was seen that phase voltage synthesization is lower when it is compared to line voltage. Hence such a factor aids in heightening of the sinusoidal curves of the waveforms. Moreover, there is no need for any form of the output filter, as the spectral performance of the line voltage is higher.

This respective article has helped in providing a new insight towards the asymmetrical variations of multilevel inverter and also helped in the establishment and the discussion of various factors and parameters related to multilevel inverters. A description regarding the advantages, disadvantages and application of cascaded H-bridge multilevel inverters has also been provided so that an idea can be established regarding the real life implementation and requirement of multilevel inverters.

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