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Cascaded H-Bridge Three Level Inverter with SVPWM Using Sample Reference Phase Voltages

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Abstract—Inverter plays an important role in the present world across the speed variation of asynchronous machine (Motor) in industries using vector and scalar control. Many researchers have proposed typical topologies among them Cascaded H bridge inverter suits to some of the applications, such as electric drives, Renewable energy sources etc. As such, among the contemporary inverter (Neutral Point clamped inverter(NPC) and Flying capacitor Multilevel inverter) exists still Cascaded H- Bridge inverter gives superior performance in terms of its modulating techniques which is unique in nature. Conventional H bridge inverter with sine PWM suffers from high THD, a novel SVPWM with sample reference phase voltage is proposed which is easy to implement and increases bus bar utilization with reduced THD in currents. In order to validate results it is implemented using MATLAB/SIMULINK environment.

Keywords: Sin pwm, Scalar control, Vector control, SVPWM.

1. INTRODUCTION

Recent developments in the power generation using renewable energy sources, variable speed drives ,and in automobile industry Inverters gained importance and to meet the present day requirement multi staggered inverter gained importance as such they provide approximate sinusoidal nature of supply to the electrical system. Conventional two level inverter has drawback of introducing harmonics with less utilization of dc-bar, to overcome the disadvantages put by conventional two level inverter staggered inverters provides better solution.

Many multi-staggered inverter topologies have been researched among them Cascaded H bridge inverter with modulation strategies have been evolved among them [1] sinusoidal pulse width inflection technique (SPM), SHE practice, Trapezoidal Recital and SVPWM are mostly used one. With the available practices SVPWM [2] offers better results in terms of THD (Total harmonic distortion). The SVPWM practice improves the eminence of waveform and at the same time proliferation of dc-bus bar exploitation which is more than 15 % paralleled to conventional SPM technique[3]. As the level of inverter increases the

complexity, mathematical analysis of SVPWM and is difficult to implement [4]. The important aspect to be pondered is trading selection of inverter states along with the subdivision design and addition of [5] inhabit times. The conventional two level inverter has only eight switching positions where as three level inverter has twenty seven switching states. Shrewdness of position[6] phase vector in terms of sector and hence the converting time calculation of power semiconductor devices is wearisome. In monitoring the speed of asynchronous machine (motor)[7] scalar control and vector control can be used. For low cost and medium power applications scalar control method is best well-matched [8]. Sine PWM intonation method for cascaded h-bridge inverter exploits the dc -bus bar voltage less when compared to SVPWM[9]. Among the prevailing PWM follows such as phase opposition carrier, phase disposition carrier are used for comparing the reference phase voltages[10] improves the nature of waveform with tolerable THD levels[11] without any improvement in Fundamental component. To increase the fundamental component [12] odd harmonic of next order(3^{rd} harmonic) is introduced[13].Three level with cascaded H bridge inverter with conventional SVPWM requires more complex calculation for the ON and Off period of the switching devices. In the proposed method SVPWM for three level inverter do not require segment control thus tumbling the time for accomplishment of procedure [14-15]with less harmonic alteration and increase in fundamental component.

2. CONVENTIONAL 3-LEVEL SVPWM FOR H BRIDGE INVERTER

3phase, 3-level H Bridge Inverter

The furthermost extreme number of line voltage levels is 2x-1 where x is the number of stage voltage levels. The quantity of line voltage levels rely upon the variation index and the given harmonics are to be dispensed with. The three -level fell inverter can combine up to thirteen-level line voltage. A set of 4 switches for each phase is used for the realization of CH-3 level inverter and is shown in the fig 1.The benefit of three-stage framework is that all the triple harmonics parts in the line voltage will be killed by 33% cycle stage move highlight. In this way, just non-triple symphonious parts should be dispensed with from stage voltage.

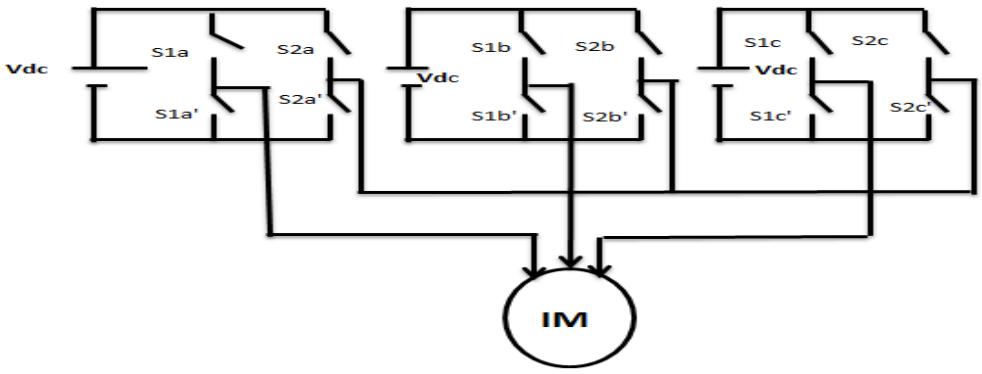

Fig. 1 CH-3 fed Asynchronous Motor

Space Vector Modulation

The conventional SVPWM uses the 3 phase voltages and converted in to equivalent two phase voltages namely alpha and beta as shown in the fig 2. Since a 3-level inverter has 3^3 states (i.e.) twenty seven positions comprising of small, large and medium vector appropriate location is identified for the synthesizing of the reference voltages as given by the equation in (1).

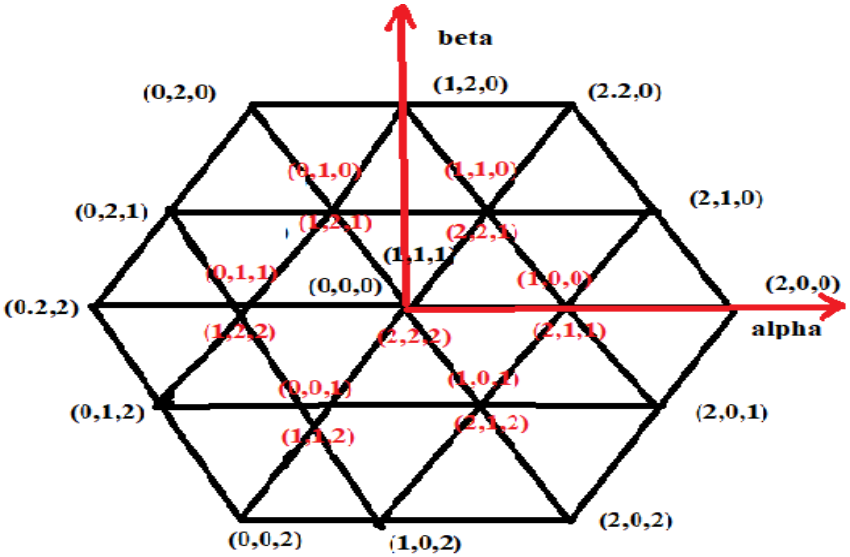

Fig. 2 Space Vector PWM in Alpha and Beta Axis

$$v_\alpha + v_\beta = \frac{2}{3}\left[v_a + v_b e^{j2pi/3} + v_c e^{-j2pi/3}\right] \qquad (1)$$

The reference voltage can lie in any region of the above mentioned states, for the proper operation of the switches an appropriate or exact of the reference voltage is to be synthesized as shown in the flow chart with calculation of m1 and m2 the general reference voltage is synthesized. The correct reference phase voltage is required and is obtained in the corresponding four regions for the sector calculation of six regions.

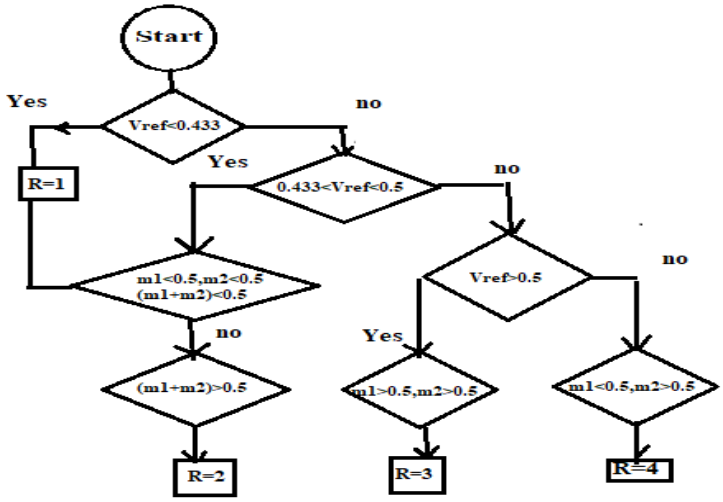

Fig. 3 Flow Chart for the Operation of Reference Phase Voltages

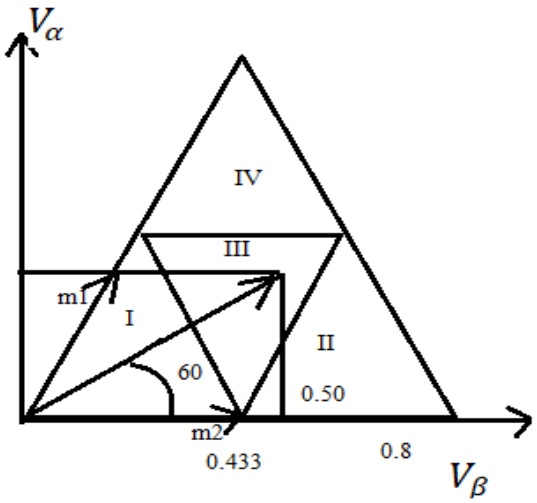

Fig. 4 Location of Sector $0<\theta<60^0$

Below are the regions as such for the $0<\theta<60^0$ the reference positional vector is subdivided in to four regions symeetrically of half side of triangle. The positional vector can lie in the above said four regions and the switching time actions for the inverter of regions are shown in Fig 5-8.

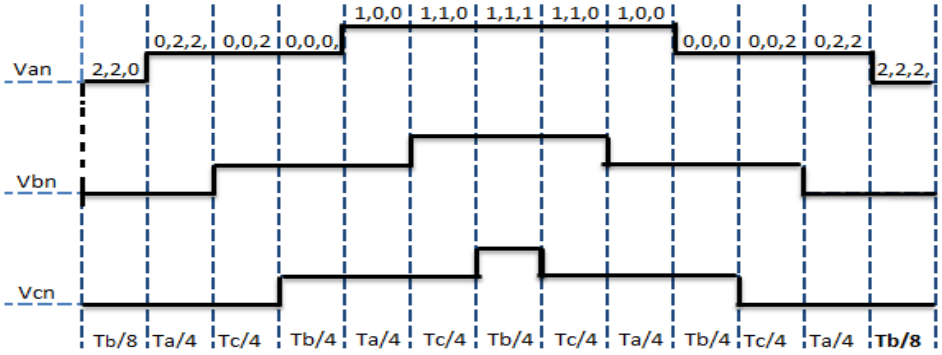

Fig. 5 Sector 1 for the Switching States of T_a,T_b,T_c

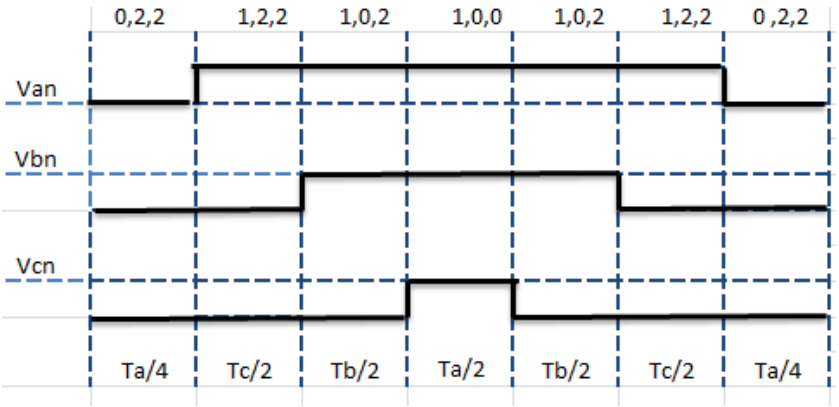

Fig. 6 Sector 2 for the Switching States of T_a,T_b,T_c

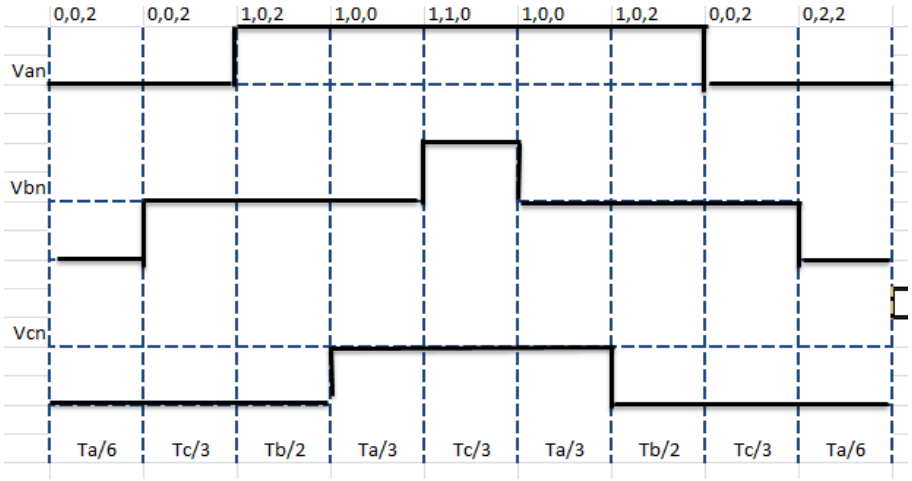

Fig. 7 Sector 3 for the Switching States of T_a,T_b,T_c

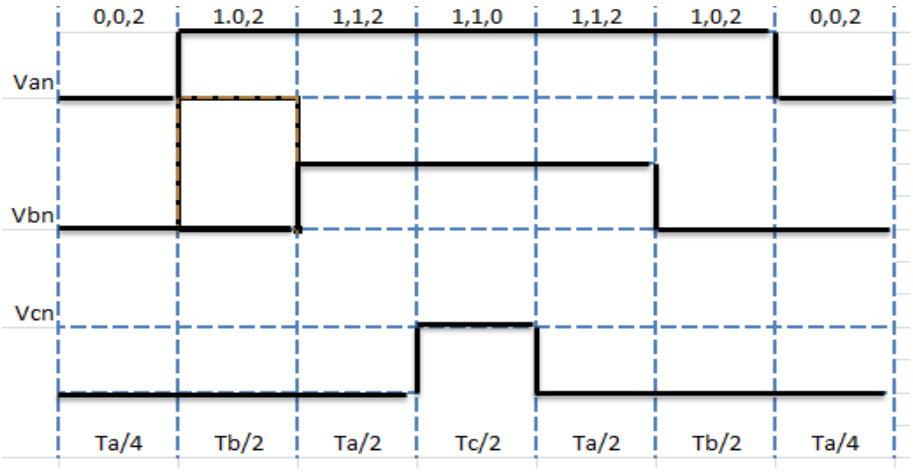

Fig. 8 Sector 4 for the Switching States of T_a,T_b,T_c

3. PROPOSED SVPWM ALGORITHM

A simple approach is made in the control of switching times for the inverter which has 12 switches. The proposed method does not require any calculation of sectors and regions it requires on the phase voltages and the offset required which added for the generation of SVPWM which contains triplen harmonics and the calculation of the switching times are as shown for different sectors can also be governed without calculation of it

Step 1	*Obtain v_{an}, v_{bn}, and v_{cn}, phase voltages*
Step 2	$T_{an} = X_{an}*Ts/Vdc/(n-1)$, $T_{bn} = X_{bn}*Ts/Vdc/(n-1)$; $T_{cn} = X_{cn}*Ts/Vdc/(n-1)$
Step 3	*Toffset : max and min of (v_{an},v_{bn} and v_{cn})/(-2)*
Step 4	Determine Carrier indices
Step 5	$T_{a\text{-}Cross} = (Ts/2)+T_{as}+((I-(n-1)/2*T_s$ similarly for other phases; I indicates carrier indices

Step 5	$T_{ga}= T_{a\text{-}Cross}+T_{offset2}$ similarly for other phases Tgb,Tgc can be obtained Where $T_{offset2}$ = max and min($T_{a\text{-}cross}$,$T_{b\text{-}Cross}$ and $Tc\text{-}_{Cross}$)/(-2)

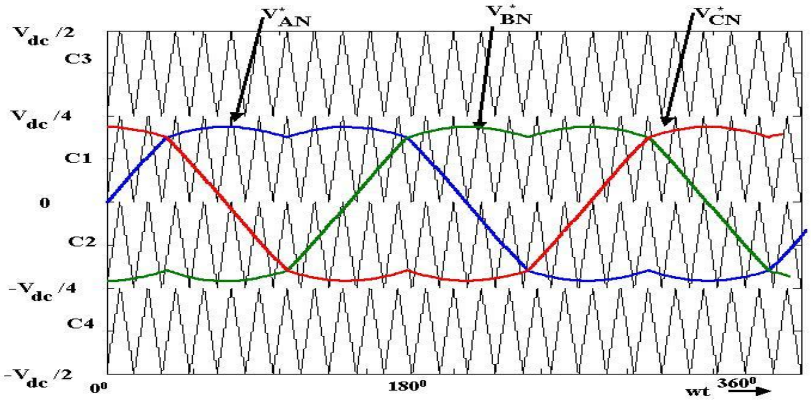

Fig. 9 Space Vector Pwm for n Level Inverter

The above algorithm is generalized for n level inverter, as such for five level inverter we require four carrier waves as shown in the above figure. 9. In the proposed method we require only two carrier waves for the generation of SVPWM .The carrier wave compares the reference phase voltage which is synthesized and obtained from the above algorithm.

4. BLOCK DIAGRAM REPRESENTAION OF CH-3 LEVEL SVPWM FOR INDUCTION MOTOR

Three phase supply is given to Diode bridge rectifier for smoothening of Output voltage suitable capacitors are used and then three independent DC voltages are obtained from the Dc output voltage which are connect in parallel across four switches of each phase so that symmetrical output voltage is supplied to all the three phase to reduce the cost and from each cell voltages are applied to the 3 phase asynchronous motor with the above algorithm which compares with the carrier wave for the generation of desired output voltages, the above method takes less duration for execution and is shown in the figure.10

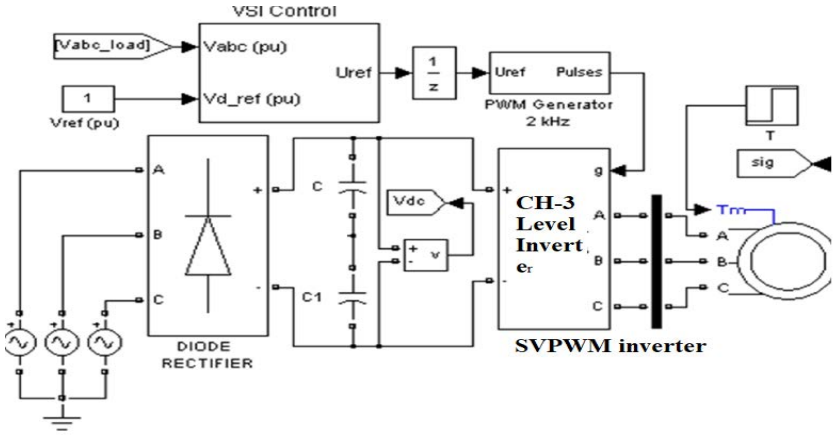

Fig. 10 Block Diagram of CH-3 Level Inverter for Motor

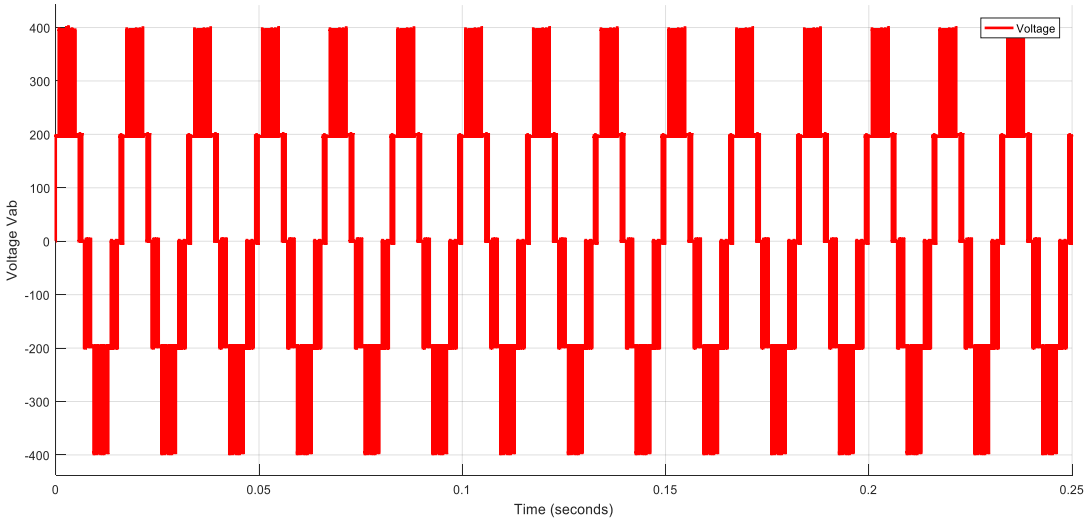

Fig. 11 Line Voltage V_{ab}

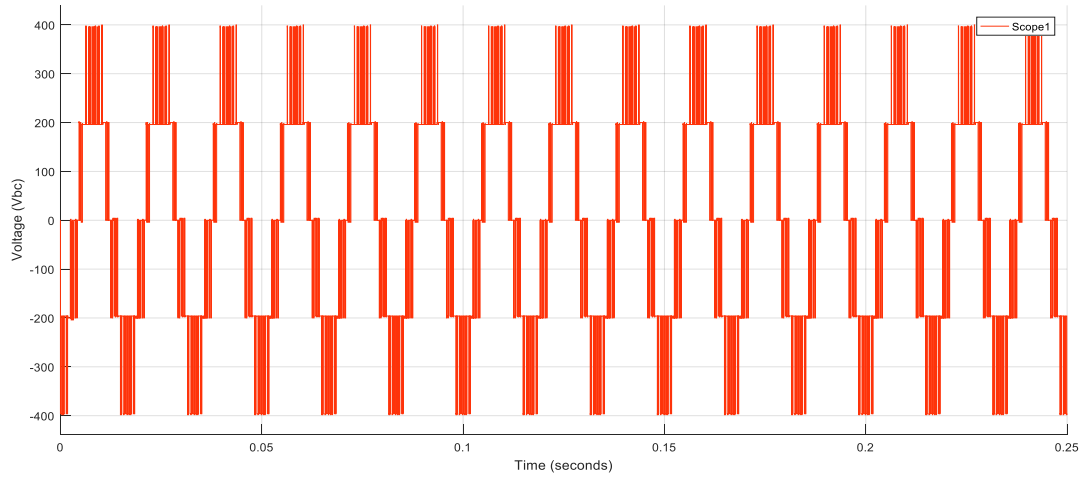

Fig. 12 Line Voltage V_{bc}

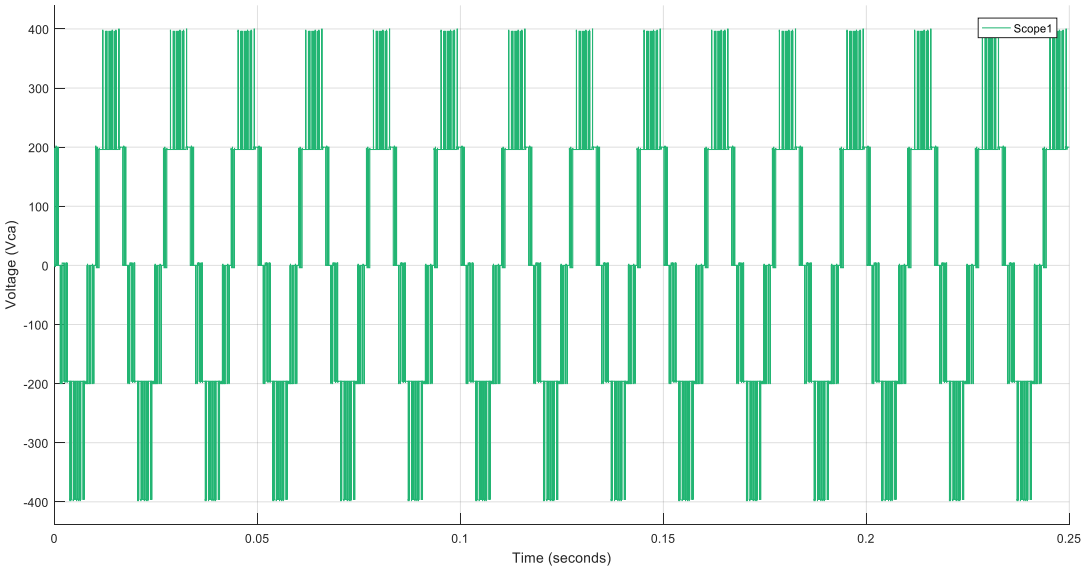

Fig. 13 Line Voltage V_{ca}

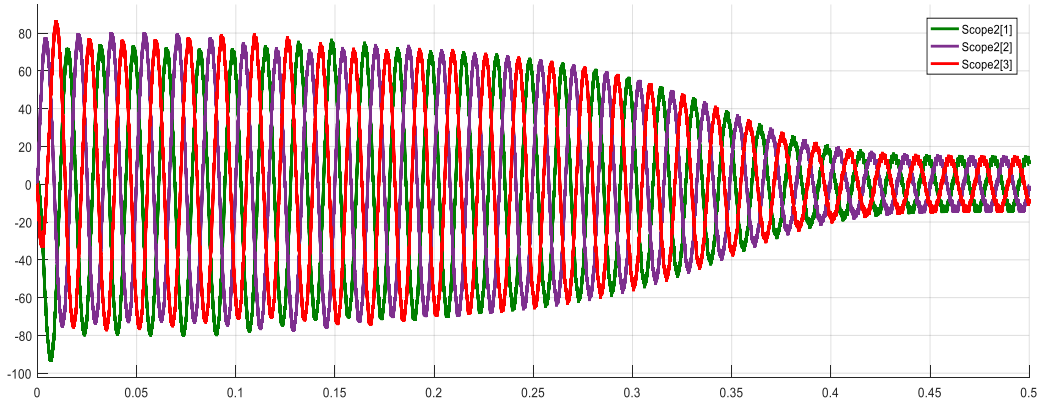

Fig. 14 Currents ia, ib, ic

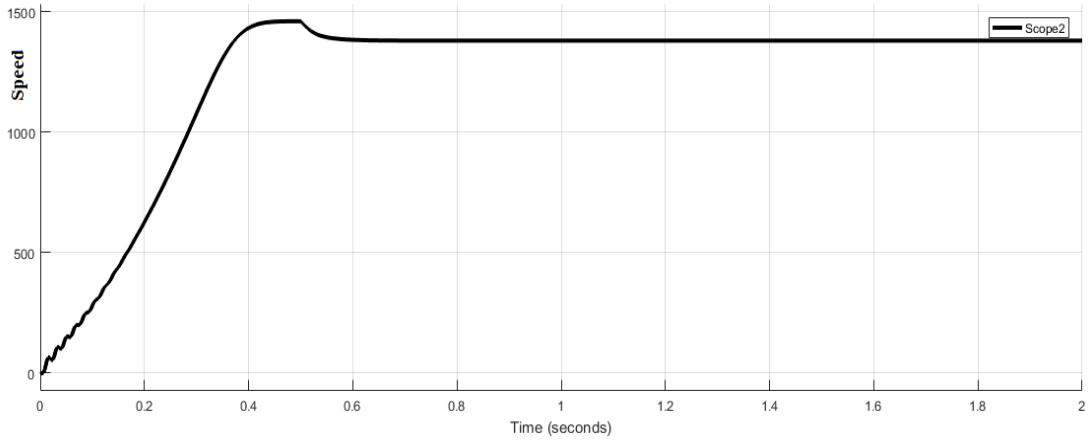

Fig. 15 Speed Vs Time

Fig. 11-13 represents the line to line voltages of Vab, Vbc, Vca, current and speed waveforms are also shown in fig.14-15 for a load of 20 N-m and exactly at .5 seconds load varies and at the same time there an increase of fundamental component of voltage which is 15% more than that of sine pwm.

5. RESULTS AND CONCLUSIONS

From the above results it is observed that implementation of new method for Cascaded -H bridge inverter shows better performance than the sine pwm and also the execution time of the above method takes less time and is simple when compared to conventional SVPWM which requires sector calculation and regions for the operation of inverter. The above technique can be implemented hardware through high end processor like DSP, FPGA.

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