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QR DECOMPOSITION FOR A LOW POWER CMOS OPERATIONAL TRANSCONDUCTANCE AMPLIFIER OPERATION

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Abstract

The purpose of this study is to investigate the benefits and drawbacks associated with applying CMFB in entirely differentiated three-stage OTAs using two loops. Specifically, the investigation will focus on determining which configuration, a single loop or two loops, yields the best results. The advantages of each method are dissected, and the ways in which they affect stability, linearity, noise, and CMR are taken into account. The results indicate that a multi-loop CMFB has the potential to enhance the filter 1-dB compression when compared to a single loop, which shows that this improvement is possible. In spite of the fact that the differential path was not altered in any way, this improvement was nonetheless accomplished.

Keywords: CMOS, CMFB, OTA, Single Loop, Multi-Loop

1. Introduction

In electrical, communication, and control systems, analog filters are an essential component that is utilized in the construction of these systems. They are accountable for carrying out fundamental signal processing responsibilities. In electronic and control systems, for instance, they can be used to filter out frequencies that are not desired, and in communication systems, they can be used to filter out the carrier signal. Additionally, in electronic systems, they can be used to filter out unwanted frequencies. In addition, they can

be used to filter out undesired frequencies in electrical systems when they are implemented [1] – [2].

The all-pass (AP), low-pass (LP), high-pass (HP), and band-pass (BP) filtering responses are the five most common types of filtering responses. All of these many forms of filtering responses are combined into a single architecture and made available through universal filters. Employing filters in which the natural frequency and quality factor can be altered independently of one another is strongly recommended. You will need voltage-mode filters that have a high input impedance as well as signal inputs that do not invert the signal in order to get rid of buffers and inverting amplifiers even further [3] – [5].

The electronic circuits that are typically referred to as oscillators are the type that is considered to be the subsequent most important. In order to generate waves with a wide variety of shapes, amplitudes, and frequencies. The term quadrature oscillator comes from the fact that these devices produce two sinusoidal signals that differ from one another by a phase difference of ninety degrees. They find widespread application, where components are dependent on their presence. If you are able to design a circuit in which the oscillation state and frequency can be regulated independently of one another, then you will find that it is much simpler to cope with whatever it is that you are confronted with [6].

The operational transconductance amplifier (OTA), which can be found in references [7], is the primary active building piece that goes into the design of OTAC filters. On the other hand, the silicon area and the power dissipation both increase when the complexity of the filter grows. Multiple-input OTAs, also known as MIOTAs, have recently come to the forefront as an intriguing new method that has the potential to reduce the number of individual OTAs required for filter design by a factor of two or more [8]. This reduction in the number of individual OTAs is possible because MIOTAs have the ability to combine multiple inputs into a single OTA. The OTA multiple inputs, which can be utilized in a variety of different ways, allow for the addition and subtraction of signals. It was stated that utilizing OTAs with multiple inputs might potentially [9].

A fantastic example of this would be the elliptic and low-pass filters of the third and seventh orders, respectively, as described in [10] and [11], respectively. However, in order to accomplish the multiple-input blocks, the MIOTAs that were used in the designs that were discussed before relied on the parallel connection of differential stages. This led to an

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increase in the amount of power that was lost, a more complicated internal structure, a rise in the number of transistors, and an increase in the total area of the chip. In addition to this, the power dissipation resulted in an expansion in the size of the chip. By utilizing the multiple-input floating-gate transistor (MIFG), we are able to construct a design that is more straightforward for the MIOTA.

In order for this architecture to function, all that is required is a single differential pair. The MIFG transistor, on the other hand, is not practicable with the CMOS technology that is currently available [12]. This is due to the fact that the MIFG transistor is dependent on charge conduction. This is because of leaking in the gate. In addition to this, the MIFG transistor has a greater voltage offset because of the residual charge that is still present on the gate.

2. OTA

One of the most fundamental components that can be found in any analog circuit is the operational transconductance amplifier (OTA). As a result of the fact that it has a high output impedance, it is intended to be utilized just with capacitive loads in order to generate a high voltage gain. This is due to the fact that it was created. Figure 1, which contains a schematic representation of the OTA circuit, by clicking this link. Numerous applications make use of the negative feedback configuration of an OTA because it makes the circuit less susceptible to process fluctuations, which in turn increases its bandwidth and linearity, lowers noise, and makes the circuit bandwidth and linearity more stable (including active filters). This is because it is mentioned in [13], which is the source of this information. These advantages, however, are dependent on the high gain that the OTA possesses in order to be realized. The amount of gain that is applied has a direct bearing on both the OTA accuracy and its capacity to ignore ambient noise.

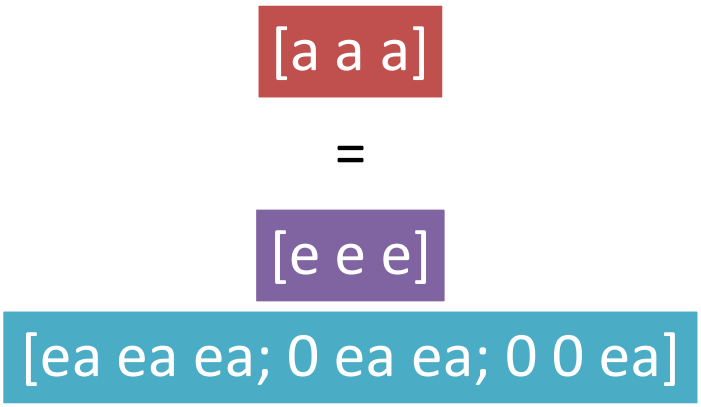

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Figure 1. QR Decomposition CMFB implementation

Common-mode feedback is utilized in a variety of distinct versions of three-stage amplifiers, all of which are seen in Figure 1. The inner amplifier is constructed out of the blocks H2(s) and H3, which also function as the component parts of the amplifier compensation network.

Because supply voltages are progressively dropped in modern process technologies, it is becoming increasingly difficult to generate high gain with a conventional two-stage OTA. This is because the supply voltages are a key factor in determining how much gain can be achieved. In addition, the conventional design for cascading places severe limits on the excursion of the signal and makes it more difficult to attain high gain. The use of several gain stages coupled in cascade, as detailed in [13, 14], is one approach that can be taken to solve this problem. In addition, a fully differentiated multi-stage OTA is required for use in high-precision applications because of its capability to reject even-order harmonic distortion in addition to common-mode noise while simultaneously increasing dynamic range. This requirement arises from the fact that a fully differentiated multi-stage OTA has the capacity to do all of these things. This capability is necessary for the successful operation of the apparatus.

Differential signaling, while it does help to improve linearity, also adds to an increase in the complexity of the circuit. This is despite the fact that it helps improve linearity. This is due to the fact that differential signaling necessitates the employment of a common-mode feedback loop, which is also referred to as a CMFB loop. This is necessary in order to ascertain the DC operating point of the amplifier and filter out common-mode noise. As a consequence of this, CMFB loops play an essential part in a variety of applications [15].

In multi-stage OTAs, the CMFB design in and of itself offers a challenge; moreover, the fact that there is such a huge range of potential topologies for implementing it adds an extra layer of complexity to the situation. The solution to the problem of the three-stage amplifier is depicted in Figure 1 in two of the many possible ways that it could be solved [16].

This is accomplished by utilizing a single common-mode feedback (CMFB) loop. This is one of the choices that are open to you. By utilizing a common-mode (CM) sensor, the CMFB loop is in a position to determine whether or not two voltages have a common-mode (CM) component. After that, the common-mode (CM) error amplifier is utilized in order to

amplify the difference between the CM component and the needed reference voltage. This is done by comparing the output of the CM error amplifier to the reference voltage. As a consequence of this fact, the negative feedback loop of the CM sensor is responsible for feeding the reference voltage into the common-mode input of the CM error amplifier [17].

In the first loop, the common-mode voltage of the H2(s) stage would be set, and the common-mode current would be fed back into the first stage output. In the second loop, the common-mode voltage of the output nodes would be set. This is one of the choices that are open to you at this time [18].

In the body of research on multi-stage amplifiers, the subject of fully-differential over-the-air (OTA) design is brought up infrequently when considering the design trade-offs associated with various CMFB approaches. This is the case when considering the design trade-offs associated with multi-stage amplifiers. If the intermediate gain stage is built totally differentially, then the CMFB loop can be constructed in a variety of distinct ways depending on the specific circumstances. Among these include the use of a single loop that integrate all three stages of the process, as well as the use of individual loops for each stage of the procedure. This is the case because of the nature of the requirement. As a direct consequence of this, access to such solutions is not available. You provide a solution that consists of two loops of switched capacitors, but you do not explain the trade-offs that have to be made in order to build these CMFB loops appropriately.

This is a problem because the approach you propose is the only one that works. It is a remarkable accomplishment in and of itself that some authors have created four-stage totally differential amplifiers by simply employing a single CMFB loop. Nevertheless, in order for their procedures to be successful, the pole of the common-mode error amplifier needs to be situated at a frequency that is noticeably higher than the bandwidth of the differential loop. In the case of amplifiers with a limited power output or applications that call for a high frequency, this may not be a viable solution. Neither of these research takes into account the impact that the CMFB loop architecture has on the linearity of the amplifier. Neither of these studies was able to find any significant correlation between the two.

Therefore, there is an urgent need for a logical strategy to deal with these trade-offs that provides designers with an idea of how good various CMFB topologies are. This is a requirement that has been around for quite some time.

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Adding unnecessary complexity in the form of extra loops would result in an increase in both power consumption and complexity, one may infer that the approach consisting of a single loop would be the simplest and most effective method to adopt in this situation. In spite of this, the goal of our work is to try to determine whether or not our first instinct was correct. With the help of a wide variety of performance standards, we will conduct an analysis that compares the two options that are now accessible from a quality standpoint. According to the findings of our research, maintaining the stability of a single loop can be difficult, and adopting a single loop may be less efficient in the long run when considering linearity, space requirements, and energy use [22].

Our theoretical and simulation-based investigation illustrates the paradoxical result that employing a large number of loops is really good for performance. This finding was reached by analyzing the relationship between loops and performance. This is especially true with regard to linearity, which is most likely the single most critical component in ensuring the proper operation of completely differential circuits.

3. Proposed Method

It is necessary that the stability of the various CMFB techniques be evaluated in a manner on the compensation scheme. This is due to the fact that there are many different kinds of compensation plans. As a result of this, if we want to make qualitative judgments about stability, we make use of the concept of rate of closure, which is abbreviated as ROC [9]. In this case study of the transistor level, two of the more typical parameters employed are called phase margin (PM), and they are settling time.

To figure out how to calculate the ROC of a two-component negative feedback loop with the equation to do nothing more complicated than plot the magnitudes of X(s) and 1/Y(s).

$$H(s)=X(s)Y(s) \quad (1)$$

The ROC can then be calculated using this information. The frequency at which the two graphs cross is referred to as the unity-gain is determined by calculating the absolute difference between the two graphs (in decibels per decade). As a result, the PM is nearly equivalent to

One of the most notable limitations of the ROC approach is that it can only be utilized for the analysis of minimum-phase systems. Because of this, it cannot be used to evaluate

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amplifiers with transfer functions, which is one of the most prevalent forms of transfer function zeros. This precludes the possibility of using it to analyze such amplifiers.

This is because the previous discussion relied on the previous factorization. The differential-mode gain is represented as the sum of the CM loop gain that has nothing to do with the actual physical circuit blocks in this factorization. This factorization is called a factorization.

The related single-loop CM circuit model for low-level signals is depicted in Figure 1, which contains an illustration of the model. The figure 1 appears as follows if we make the assumption that AEA fully absorbs the transfer function: It is predicted that the stages of the inner amplifier will make use of the transfer function H(s)=H2(s)H3, and it is also anticipated that the loading impact of the compensation network will be accounted for in Z1. These two things are expected to happen (s).

The operation of the transfer function When modeling an AEA, the inclusion of at least one pole is required for accuracy.

AEA(s)=AEA(0)1+s/ωCM, (2)

After that, you can figure out the gain of the CMFB loop by applying the following formula.

LCM(s)=−gmCMZ1·H(s)·AEA(s) = −ADM(s)·AEA(s)·gmCMgm1, (3)

The gain in this mode is a transfer function of order 3, and it is represented by the notation ADM (s) = gm1Z1H. This is due to the fact that there are three stages in the differential path (s). It is necessary for the gain of the CMFB loop to be of at least the fourth order in order to accommodate the presence of at least one pole in the AEA(s).

An analysis of the ROC requires the construction of a graph in which the magnitudes of ADM(j) and [AEA(s)gmCMgm1]-1 are displayed along the same axis. This allows for the analysis to be carried out. Finding the point where the two graphs meet is how the crossover frequency is calculated; this is the intersection point.

The ROC for the worst-case scenario is -80 dB/decade, which can be shown in the picture. This implies that the PM is within the negative region. An increase in the PM is the consequence of increasing the speed at which the CM error amplifier runs, as demonstrated by the curve with the dots. In the second situation is compatible with a PM value of zero (marginal stability). A ROC of 20 dB/decade has the potential to increase the phase margin

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to approximately 45 degrees, but that in order to achieve this ROC, the CM loop must be significantly slowed down.

The addition of a compensation capacitor CCM and a buffer is required in order to implement the method of compensation that has been proposed for this scenario. Because of this, the pole (CM) of the CM amplifier is not defined by a much more minute parasitic component but rather by the compensating capacitor. This is a direct result of what has just been stated. The buffer is included in the circuit so that the differential mode loop can be isolated, and so that the compensating capacitor won't fill up with load. It is vital to keep in mind that the Miller effect can be used to make do with a smaller actual capacitor by picking the output of H2 rather than its input for compensation. This can be done by making the selection for the compensation. If you do that, then this will become possible.

The formula for calculating gain in the CM loop is as follows:

$$LCM(s)=-gmCMZ1\cdot H(s)\cdot A'EA(s), \quad (4)$$

Demonstration illustrating the effect that the loading from the compensating capacitor has on the bandwidth As a consequence of this development, we can at long last commit our ideas to paper.

$$LCM(s)\simeq -gmCMgm1\cdot ADM(s)\cdot A'EA(s). \quad (5)$$

The bandwidth had to be reduced in order to accomplish this goal. In order to provide a monetary value to the narrowing of the bandwidth, we must first determine the point from 40 dB/decade to being 20 dB/decade.

$$20\log\omega'CM = 20\log(\omega pd\omega'CM) \quad (6)$$

4. Results and Discussions

The power consumption and voltage gain as a function of the change in supply voltage are represented graphically in Figure 2, which can be found here. To be more exact, it can be demonstrated in Figure 2 that the voltage gain raises in an exponential fashion as the supply voltage lowers, all the way down to approximately 400 mV, where it stabilizes. This is the case even though the supply voltage is decreasing. As shown in figure 3, the efficacy of the voltage gain approach that makes use of the upgraded composite transistor decreases as the

supply voltage is raised. This is demonstrated by the fact that the effectiveness of the technique is shown to decrease. This is a fact that can be witnessed for oneself.

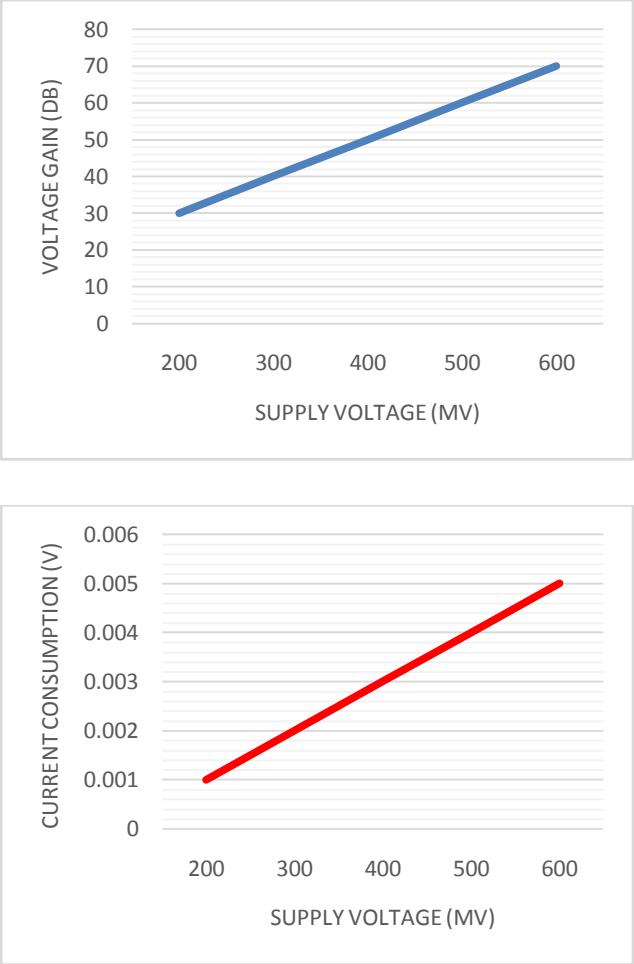

Figure 2: Voltage supply dependence

Figure 2 presents a graphic representation of the connection that exists between the supply voltage, the gain-bandwidth product, the total current consumption (IT), and the voltage gain (GBW).

Gain-bandwidth product (GBW) and current usage are shown in Figure 1b as a function of the fluctuation in supply voltage. Additionally, the relationship between the two variables is illustrated by this picture. The power consumption of the OTA increases exponentially with the supply voltage, as does its gain-bandwidth product GBW. This is due to the fact that the inverter transconductance Gm for the weak inversion operation is connected to its current consumption [21,22]. This is due to the fact that the inverter transconductance Gm is proportional to the amount of current that it consumes.

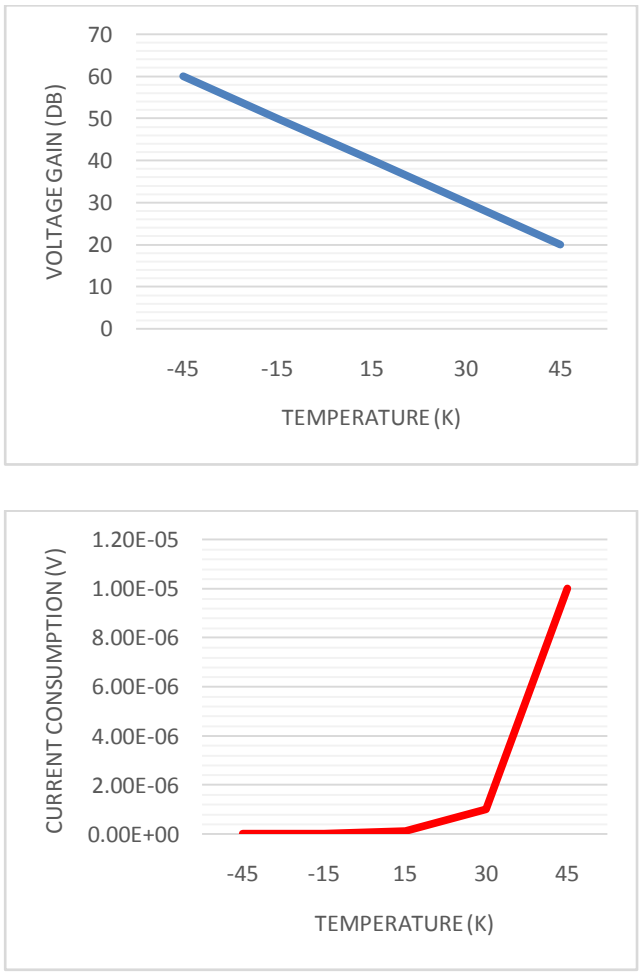

Figure 3. Temperature dependence

Figures 3a and 3b illustrate how the voltage gain and power consumption of a 0.3 V voltage source change as the temperature changes.

It has been demonstrated that temperature has an effect on each of these variables. As the temperature rises, it is clear from equations (6) and (7) that the voltage gain suffers a sizeable loss, along with a fall in GM, and this loss is proportional to the increase in temperature (4). In addition, as the temperature rises, the threshold voltage drops, which results in an increase in the total current and, as a direct consequence of this, an increase in the GBW.

The link between temperature and the gain-bandwidth product, total current consumption (IT), and voltage gain is depicted in Figure 2. (GBW).

The input-output characteristic of the proposed OTA is depicted in Figure 3a and b, together with the OTA gain vs the output voltage for the case when VDD = 0.3 V. The

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corresponding results for VDD = 0.6 V can be seen in Figure 4a and 14b. Figure 5a and b show the OTA gain in relation to the output voltage when VDD is set to 0.9 V. Because of the reverse transistor current and channel length modulation [22], the output voltage has an impact on the OTA voltage gain, as shown in Figures 13b and 14b. This is the case because of the channel length modulation. The consequence of this is that it causes corresponding fluctuations in the output conductance (go). As a result of this, the proposed OTA has the potential to cause output voltage fluctuations of 100–500 mV at VDD = 0.6 V, assuming that the gain AV is more than 30 dB. These voltage swings could occur at any time throughout the operation of the OTA. PMOS or NMOS transistors, depending on the design, are used to apply the output range limitation by transitioning into the linear zone outside of the stated limitations. The peak of the voltage gain occurs at approximately half of VDD in the input when VDD is equal to 0.3 V, and the behavior of output conductance changes accordingly. The current that is passing through the reverse transistor is what controls the Go setting. In any over-the-air (OTA) application that utilizes feedback circuits, the voltage gain should be high all the way throughout a broad output voltage range in order to provide excellent signal linearity. This is significant because the small-signal voltage gain can give an incorrect impression because it only displays the greatest voltage gain.

Table 1 presents the outcomes of the simulations that were carried out in each of the four corners of the room. The corners have the most intrinsic input offset since the size of the inverter transistor was created for the typical corner TT. This resulted in the corners having the largest intrinsic input offset. As was previously established, the frequency of the input signal as well as the gain bandwidth each have a unique effect on the linearity of the OTA. Together, these two factors may be broken down into four categories: (GBW). It would be possible to use more biasing circuits [21] or calibration [27] in order to lower PVT variability, which would ultimately result in more consistent performance.

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Table 1. GBW

VDD (V)	Power (nW)	GBW (kHz)
0.1	0.276	0.211
0.2	41.178	15.100
0.3	0.093	0.071
0.4	14.079	5.240
0.5	0.428	0.341
0.6	68.943	25.604
0.7	0.332	0.243
0.8	44.521	15.403
0.9	0.801	0.621
1.0	118.675	42.915

The results of one thousand separate runs through the Monte Carlo simulation are summarized in Table 1, together with the values for the Mean and Standard Deviation. Mismatches and process variations are each explored on their own as well as in conjunction with one another. The results of an out-of-band analysis (OTA) lend credence to the hypothesis that the degree of process variability has a substantial bearing. This is because the findings show that the degree of process variability has a substantial bearing on all three of these variables (P).

There is not a significant change in the power efficiency Figure of Merit, also known as FoM, which is defined as 100 (GBWCL)/IT. This is because there is not much of a change in the power efficiency. In a manner analogous to this, there is no change to the open-loop voltage gain. The fact that the mismatch variations have a significant impact on the offset voltage VOS of both OTAs is a significant issue that has to be resolved as soon as possible. The input offset voltage for the 3 mismatch variation is found to be 8.7 mV when VDD is equal to 0.3 V, and it is found to be 8.9 mV when VDD is equal to 0.6 V in the simulations.

Table 1, which has been tabulated for your convenience, provides a summary of the potential outcomes of the OTA as well as comparisons to alternatives that are considered to be state-of-the-art. Contemporary OTAs can be divided into two distinct categories: gate-driven and bulk-driven, with the distinction between the two being based on the type of

drive that is connected to the input terminal of the first-stage amplifier block. Each variety comes with both positives and negatives to consider. Even while the bulk-drain transconductance is much lower than the gate-drain transconductance, gate-driven OTAs have a broader voltage input range, which results in less signal distortion at higher voltage signal amplitudes. This is because the gate-driven OTAs can accept a wider range of voltages. However, this is not the case for bulk-driven OTAs because the values of their transconductance are in the other direction.

Even though these kinds of circuits have a larger footprint and consume more power, they are preferred in a variety of settings because the voltage range is better and there is less distortion. This is because these kinds of circuits have a less amount of distortion.

The over-the-air transmitter that has been proposed is unique in a number of respects, including its voltage gain as a function of the number of stages, its small size, its high power-efficiency figure of merit, and its good linearity in relation to the input voltage. All of these characteristics contribute to the over-the-air transmitter overall appeal. It is possible to increase the voltage gain by including additional amplifier stages; but, doing so would need more physical space and make it necessary to include a stability compensation circuit.

In [21], there is a presentation of a power-efficient design that has 1020 FoM and 0.3 V as its supply voltage. You may view the document by clicking here. The new design has a FOM of 229. This is 4.45 points less than the old design FOM. On the other hand, while the former has a THD of 3% for a signal with an amplitude of 100 mV peak-to-peak, the latter only has a THD of 1% for a signal with an amplitude of 120 mV peak-to-peak. This difference in THD is due to the fact that the latter has a higher signal amplitude. Despite the fact that it only has a single stage of gain, the voltage gain of this cutting-edge device is second best among those that work on sources of less than 0.3 V. This is the case even though it only has one step of gain. However, due to the fact that it is a multiple-stage OTA design, it has an area that is 25 times larger. The proposed OTA would have a voltage gain of 40 dB at the same source voltage of 0.25 V, whereas the best voltage gains under 0.3 V supply voltage [32] is 60 dB. Despite having a supply voltage of only 0.4 V, the [18] has the highest voltage gain of all OTAs, coming in at 81 dB. This is despite the fact that it has the lowest supply voltage. The suggested OTA only requires one gain stage in order to achieve a 66 dB voltage gain at 0.4 V supply voltage while taking up approximately five times less area than the alternative.

The inverter-based OTA that is presented in [21] serves as the comparison that is most applicable because both versions were constructed for the same process and have the same size transistors and voltage supply. In addition, the comparison that is most applicable is the one that is presented in [21]. The FoM power efficiency is nearly half as great as it is when VDD is equal to 0.3 V, but the input voltage excursion is 3.4 times as large for the same total harmonic distortion. Moreover, the total harmonic distortion is the same (THD). In addition, in contrast to its predecessor, the voltage gain of this model has been subjected to a few modest modifications in order to improve it.

5. Conclusions

A single CMFB loop can be the first thing that comes to mind for the designer when thinking about how to build a fully OTA. This can add a significant amount of expense and complexity to the design, so it important to be aware of this potential pitfall. The performance of both methods in terms of noise is equivalent. This is because the multi-loop technique allows for more control over the feedback loop. This is because the loosening of these limitations will allow the single-loop implementation to use a smaller feedback loop. In the event that the design was not intended for high-frequency operation, this will be the result (albeit at a decreased bandwidth). Even though this study does not make any assumptions regarding topology, there may be other qualities that need to be taken into consideration when choosing which kind of CMFB implementation to use. One of these characteristics is power supply rejection, which is heavily influenced by the construction method of the transistor.

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