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Implementation Of Xor Based Multiplier Using Mux

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Abstract: A novel self-pipelining technique is developed in this work. Which includes proper synchronization between the stages for high-speed and low-power multiplication is defined. To accomplish the proposed self-pipelining process, the true and complementary clock inputs are added alternative to each corresponding self-latching step. First was designed a 4-b×4-b self-pipeline Wallace-tree multiplier based on the above idea. The key purpose of our proposed approach is to minimize the amount of transistors relative to the current system such that we build circuits where the complete adder is made of multiplexer depending on XOR that is used in multiplexers. Comparing between the current competitive designs to our proposed design shows that supremacy results.

1. Intoduction

Now a days VLSI developers desire to develop two parallel architecture [1-3]. Multiplication performs as a crucial bottleneck to enhance the productivity of many other computation-intensity electronic innovations by speed-power. A lot of experts are researching to increase the accuracy of speed-power for parallel multiplier, but this can be demonstrated in [4-15]. n Conventional Register-Pipelining [12] will provide enhanced digital multiplier high throughput efficiency and increased in power, region and total latency [6]. In addition, the unregulated (produced) clock-skew at various moments can also trigger device breakdown. A further challenging task is register pipeline method [6-7] is to design clock-driver.

Ever since C.S. Wallace introduce a parallel multiplier, In 1964[22] then later, by L. Dada was researched in 1965[23] to accomplish high-speed multiplication along with low-power dissipation, a series of structural modifications. Quick technology advances in conventional MOS systems on a nanoscale and enhanced feature / device density in a single monolithic IC often create durability is a major layout concern. Raising feature intensity with complicated interface connectivity contributes to localized heat (hotspot) generation which is essential for increasing the amount of IC failure[24].

From the other hand Wave-pipelining [6-7,16], by removing intermediate latches / registers from the circuit, can minimizing the risks associated with conventional register-pipelines. The large throughput in wave-pipeline method does not rely heavily mostly on critical phase latency though on the interruption variation between the longest and shortest path delay[16].Area, power and latency of register pipelines can be removed from this concept. Further information can be found on wave-pipelining in [6-7,16]. Even so, the time / delay equalization between all the data paths from inputs and outputs is incredibly crucial for enhancing speed-power efficient wave pipelined system. The leaf-cell level data-based delay [6-7] has a significant part in achieving efficient time-equalization. In addition, the impact of the PVT (Process Voltage Temperature) will give towards unstable wave-pipeline system [16]. Basically, the performance of a wave-pipeline device is mostly based upon this developer abilities.

This research suggests a modern self-pipeline approach which can boost efficiency and durability in terms of speed-power relative to register-pipeline and wave-pipeline architecture for digital circuits / systems, respectively. Developed self-pipeline framework as described in [15] was developed on the basis of self-latching methodology. The total structure is split into self-pipeline steps and enabled and disabled at each step of the system utilizing clock input in the consequent duration creating new pipeline strategy.

At first a 4-b×4-b multiplier has been designed based on proposed idea. In our proposed idea where the full adder is made of XOR based multiplexer which is used in multiplier is explained below sections.

2. Literature Survey

M Ahmed. Shams et al.[17] proposed adder unit that had been separated into 3 constituent modules . Specific prototypes were introduced for every of those units. This results in power usage, less latency and throughout the simulation, and need to work done on intermediate buffer insertion during the simulation. Jin-fa lin [9] proposed a reducing method of difficulty in the circuits on semi-dynamic latch-adder cell is implemented. The layout is economically most powerful in all models, as well as provides the smallest layout area. Which results in reduced power consumption however the smallest layout is required.

Chip-hong chang et al. [18] proposed High energy output across a large spectrum of input voltages. The combined amounts and outcomes often give tremendous consistency in the distribution. p.Burleson [13] Modern technologies prefer with intensity and pace at the expense of broad variance of parameters. The utilizing of synchronous system techniques is only solution. Does have benefits in power consumption and low latency.

P. Ramanathan et al. [11] proposed New technique of digital multiplier implementation using decomposition logic. The overhead costs of pipeline implementations and multipliers are faster and faster. That makes for high power and less delay.C.S. Wallace [14] proposed Machines that are very complex and hard to construct without the look-head buffering through memory and arithmetic that results in speed consumption however it needs high cost.

Jin-fa-lin et al. [20] proposed The designs of the carry sum module are composed of two multiplexing frameworks only with 5 transistors, that minimizes power and area and therefore it requires increase speed. Sanjeev Kumar et al. [16] proposed A 4 * 2 compressor circuitry depends on the current XOR, xnor design was proposed which offers better power consumption efficiency advantages. Dalai gowri sankar rao [21] proposed This compressor method could be chosen for low-power electronic circuits.5 * 2 compressors relying on a high-speed, low-power, XOR,xnor gate and multiplexer made from transmission gates. k.Hari Kishore et al.[22] For high speed output a novel transistorized 8 * 8 multiplier was added. Concluded that the methodology of compressor 5 * 2 is stronger than that of compressor 4 * 2 even without compressor methodology.

V. Gupta et al. Conventional MA(mirror adder) cell's complexity by reducing transistor no. and load capacitance. A decline in the amount of transistors connected to the series has managed to decrease the successful switched capacitance and achieve voltage scaling that benefits from a very minimal loss in performance quality. g.oklobdzija [23] proposed A method was proposed for implementing a speed-optimized multiplier tree which includes a net list generation algorithm. Globally optimized to produce slices of vertical compression in dividual form.

Kazuo yano [24] proposed Due to the lower input capacitance, the power dissipation is also smaller. Multiplication of floating points by carefully optimizing architecture of multipliers for high speed operation. Padma balaji RD [25] proposed Adder provides performance at high speed with delay. To boost the efficiency, dual threshold may be introduced in architecture. That results in less area and less power usage. Urinda [2] proposed Small increase in area and power but time delay is lower than conventional wallance tree multiplier resulting in high speed but high circuit complexity and time delay need to be reduced.

3. Existing Work

Transient answer checked via the AND gate via the circuit working of the 2-input system, seen in figure. 1. As seen in fig.1, the AND circuit is elevated to "EN" and retains its value when "EN" input is small. The

"ENB" input is a complement to the "EN" input and is seen in the figure. The images of the self-attached Full-Adder and its moving response to the T-Spice are seen in Fig.2 and Fig.3 respectively.

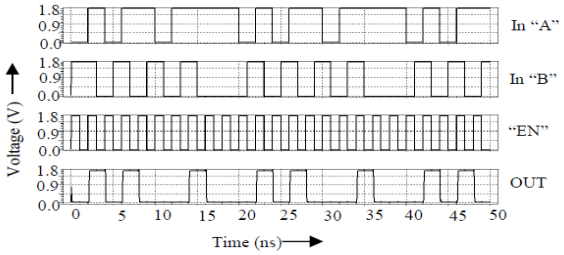

Fig. 1 Transient response of Latch-AND

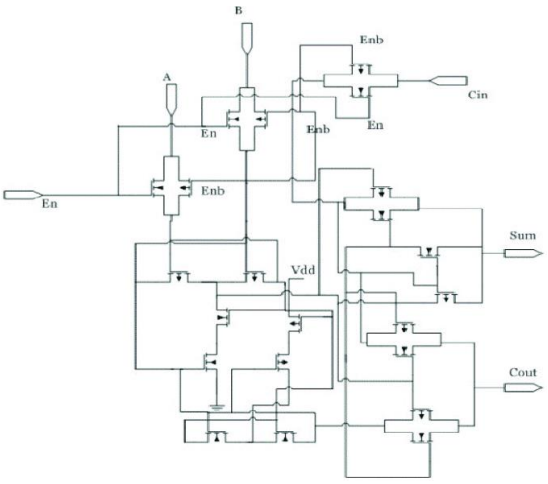

Fig. 2 Existing self-latching Full-Adder Schematic

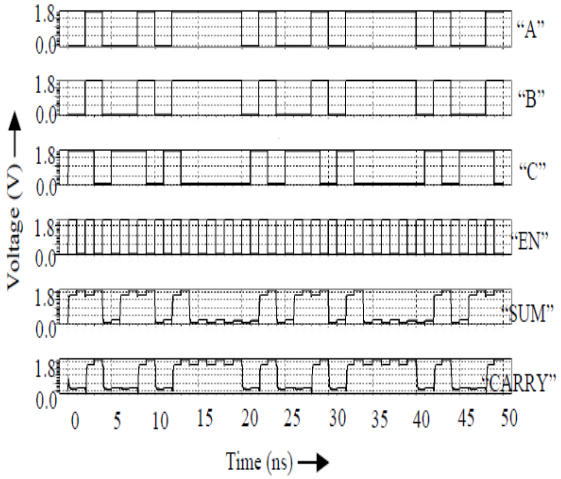

Fig.3 Transient I/O response of self-latching Full-Adder

The full-adder, as shown in Fig.3, comprises of three sources, "A," "B" and "C." Two complete adder outputs are "Total" and "Bear." The self-adjusting adder suggested confirms the transient response functionality (Fig.3). The concept above was taken advantage of to build other leaf cells for the planned self-pipeline multiplier. Figure 4 displays the design configuration, which is 4b to 4b self-pipeline.

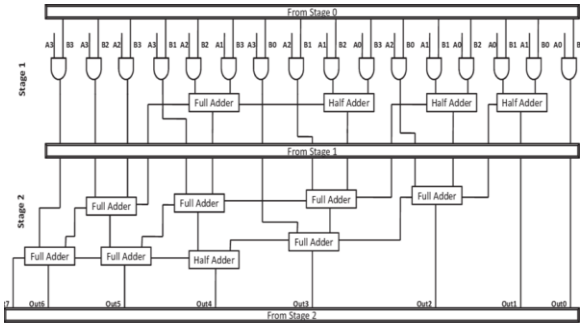

Fig.4 Existing 4-b×4-b Self-pipelined multiplier Schematic

In this circuit used in 24 transistors. In order to reduce the number of transistors from above circuit we are implementing a novel method multiplier using XOR based mux in a full adder.

Some of the binary adders are summarized in this section. The most basic simple adder is the Ripple Carry Adder (RCA)[3][4] but it is the slowest with O(n) area and O(n) delay, where n is the operand size in bits. Carry Look-Ahead (CLA)[5][6] have O(n· log(n)) area and O(log(n)) delay, but typically suffer from irregular layout. An area efficient CLA is proposed by the authors in [7].

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4. Proposed Method

Proposed 4b*4b Multiplier in XOR based MUX:

To this design the proposed 4b*4b multiplier here we are replacing with XOR gates in multiplexer which results in reducing in power, area, delay and transistors.

To reduce power by using minimum number of transistors in full adder circuit where the full adder is made of XOR based multiplexer which is used in multiplier.

XOR based MUX:

Control or selection input which depends on combination circuits which consists of many numbers of input data and single output. Such as N input lines, log n (base2) selection lines, or we might say n selection lines are required for 2n input lines. "universal logic circuit, many to one circuit or data n selector, parallel to serial converter these are also defined by multiplexer. In order to increase the amount of data which is sent over the network that consists amount of amount of data for this purpose we mainly use multiplexers.

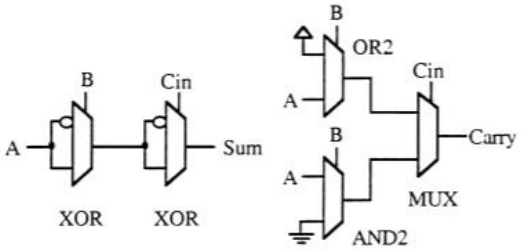

Fig. 5. Sum and carry based on 2-1 MUX circuits

All modern adder architecture designs are determined by 2-1 MUX circuitry. Such circuits are being used as basic building components for implementing of the adder. Every single MUX executes a specific role as shown in Fig. 5.
While utilizing 2-1 MUXs to develop a full adder as compared to executing every logic feature directly, it is possible to remove multiple inverters that are otherwise necessary to produce complementary inputs. As a consequence, the cumulative amount of transistors to MOS can be reduced.

Full adder realization predominantly using 2:1 MUX:
The most crucial component among processor is 1-bit full adder which determines its throughput and this is used in ALU and floating-point unit, cache or memory access for the address generation[12]. Thus, it is inevitable that full adders have a major effect on the devices utilizing these adders. Use XOR and multiplexer in yet another complete adder style. XOR gates are the most energy-hungry components in cells with complete adder. Thus, the new approach to logic will reduce the power consumption.

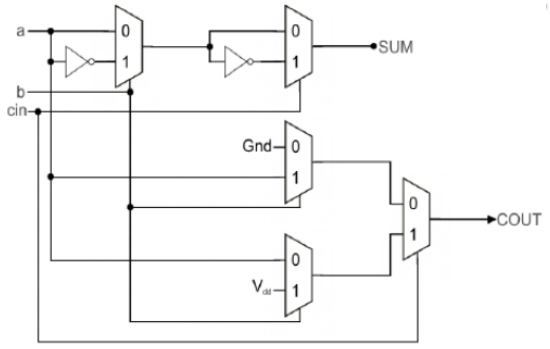

Fig 6 : Full adder realization predominantly based on 2:1 MUX

This XOR gate based on multiplexer lessens transistor counts. The multiplexer is constructed only using two pass transistors. The existing conventional CMOS has 26 transistors full adders where as our proposed full adder circuit based on XOR gate which consumes less number of transistors.

5. RESULTS

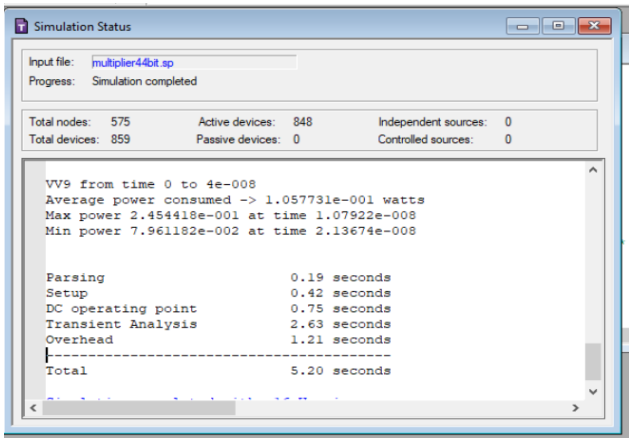

Fig 7: 4-Bit full adder simulation

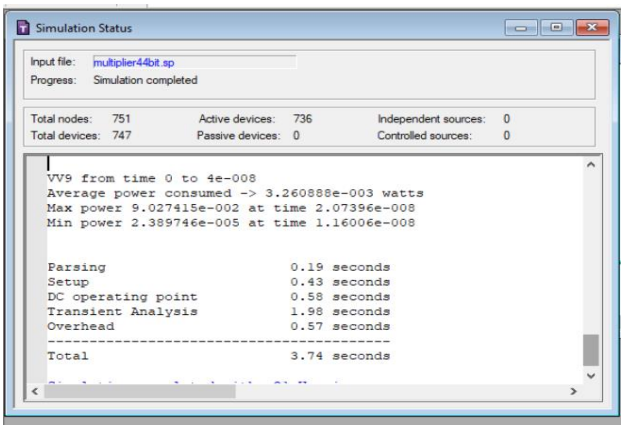

Fig 8: 4 bit XOR based multiplier simulation

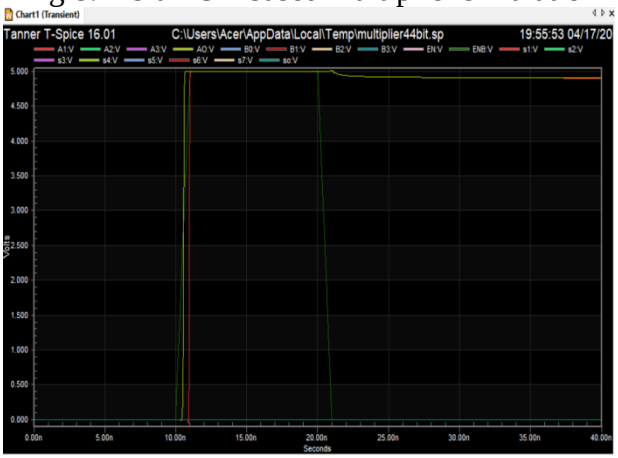

Fig 9:4 bit multiplier waveform

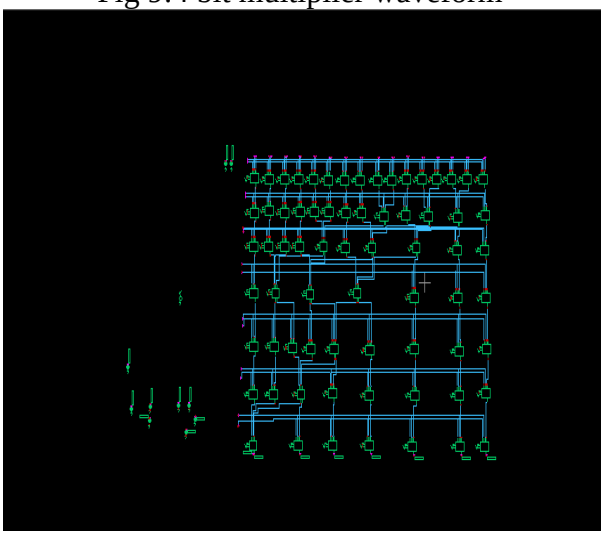

Fig 10 : 4-bit multiplier schematic

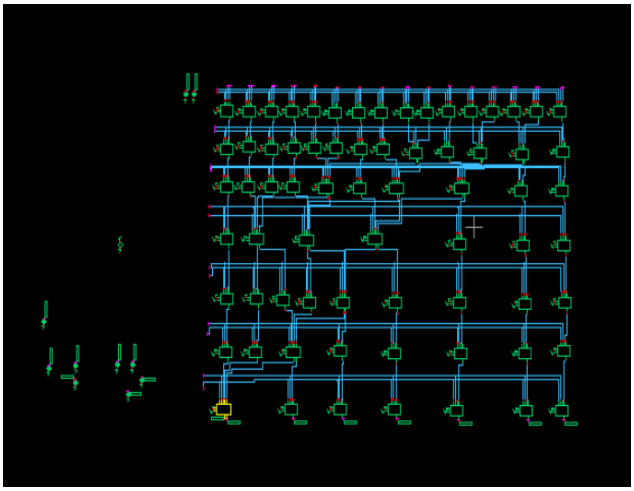

Fig 11: 4-bit XOR based multiplier schematic

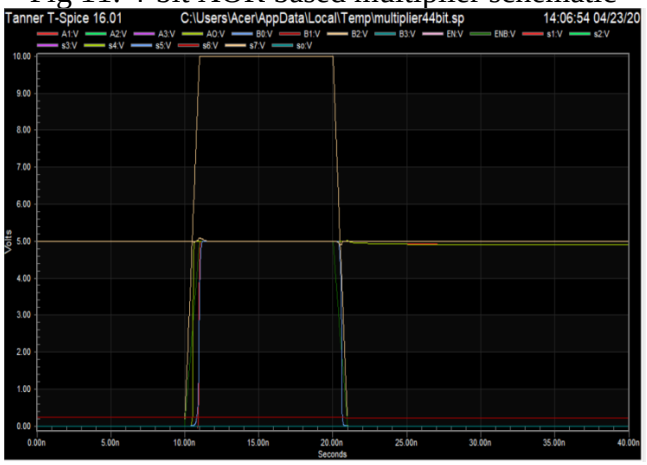

Fig 12 : 4-bit XOR based multiplier waveform

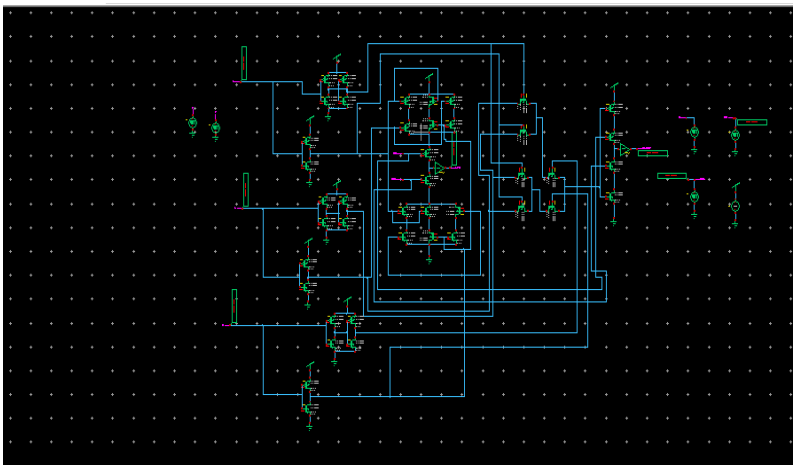

Fig 13 : Full adder schematic

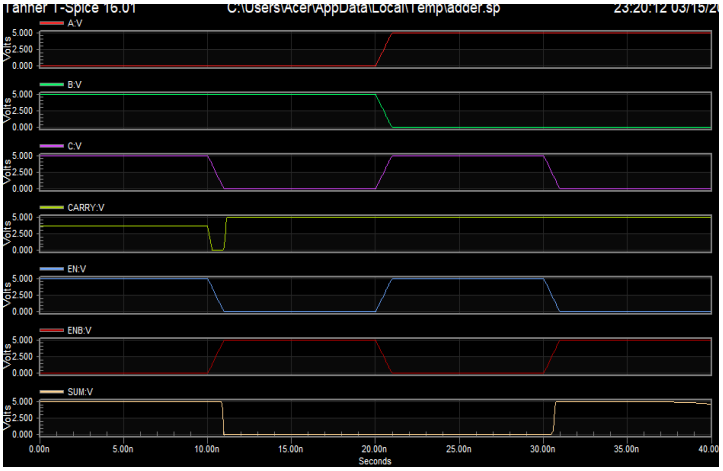

Fig 14 : full adder waveforms schematic

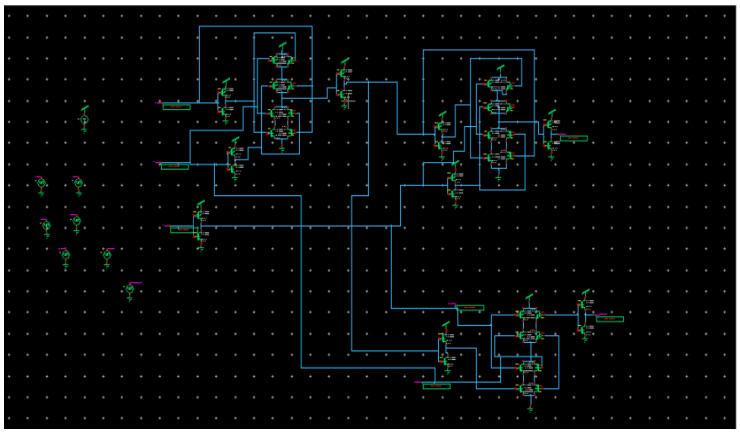

Fig 15 : XOR based multiplier schematic

Comparision Results:

Existing work	Proposed work
Power Results	VV9 from time 0 to 4e-008
VV9 from time 0 to 4e-008	Average power consumed -> 1.057731e-001 watts
Average power consumed -> 3.507989e-003 watts	Max power 2.454418e-001 at time 1.07922e-008
Max power 1.033042e-001 at time 2.06827e-008	Min power 7.961182e-002 at time 2.13674e-008
Min power 2.044020e-005 at time 1.15708e-008	
Parsing 0.19 seconds	Parsing 0.19 seconds
Setup 0.48 seconds	Setup 0.42 seconds
DC operating point 0.55 seconds	DC operating point 0.75 seconds
Transient Analysis 2.36 seconds	Transient Analysis 2.63 seconds
Overhead 1.59 seconds	Overhead 1.21 seconds
Total 5.17 seconds	Total 5.20 seconds

6. Conclusion

A new self-pipelining technique is built in this paper with XOR-based MUX that reduces transistors resulting in improved speed-power efficiency. Half adder, XOR based MUX, developed in this circuit with And gate. proposed structure is generated by using self-latching leaf cells. From this concept the register-pipelining and wave-pipelining and their associated problems have been reduced. 4-b×4-b pipelining multiplier uses decomposition logic. Comparing of speed-power performance of proposed design 4-bx4-b self-pipelined multiplier with current competitive layouts which results superiority of our proposed concept.

7. REFERENCES

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