

Implementation of negabinary number calculation using digital system design

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Abstract

There will most extremely transport exchanging action in the ordinary two's supplement portrayal of information, due to the sign expansions in the higher- request bit positions. Utilization of marked digit portrayals can limit this impact. A negabinary portrayal lessens information transport changing movement to a degree practically identical to that is given by the better-known sign-size documentation.

Keywords: Negabinary, Power Dissipation, Adder, Subtractor, Digital System Design.

1. Introduction

The utilization of negative base for speaking to numbers in advanced frameworks, was recommended as ahead of schedule as 1957[1]. The benefits of utilizing negative-base number juggling were talked about broadly in [6]. Different papers managing this subject have been distributed in recent years [1-13]. This paper is worried about the advancement of another kind of viper which is less difficult than those proposed by [4] and [12], and with the usage of the fundamental math tasks utilizing this snake.

This paper presents another binary number calculation and design that utilizes the blended negative double framework, which applies a weighted- moved [19],[20],[21] expansion idea to perform deduction. Likewise, an equal exhibit augmentation plot is proposed dependent on the external item idea. In this way expansion, deduction, and increase can be acted in one stage without the requirement for sign digits, conveys or recoding for both positive and negative numbers. A two-phase cluster design for computerized complex augmentation can be accomplished by the mix of four preparing exhibits into one composite cluster. This paper presents another math calculation that utilizes the blended negative twofold framework, which applies a weighted-moved expansion idea to perform deduction. Likewise, an equal cluster increase conspire is proposed dependent on the external item idea. In this manner expansion, deduction and duplication can be acted in one stage without the requirement for sign digits, conveys or recoding for both positive and negative numbers. Two-phase exhibit engineering for computerized complex augmentation can be accomplished by the mix of four handling clusters into one composite cluster.

2. Advantages of Nega binary System

Negabinary number system has the advantage that it can be used for both positive and negative numbers. Arithmetic circuits like adders and subtractors [1], [2] A/D conversion and many complicated arithmetic operations like division and square rooting are design using negabinary number system Now a days negabinary number system is also use in digital optical computing [22],[23],[24]and in the designing low power circuits [18]. The algorithm developed for converting the binaty to negabinary has made the use of negabinary number system more popular. The negabinary number system is also very effective in binary serial operation. Another advantage of negabinary number system is it will the circuit is design using negabinary number system.

3. Nega Binary Adder and Subtractor

Let m be represented by the bit pattern

$$(m)_2 = (.. m_6 m_5 m_4 m_3 m_2 m_1 m_0)_{-2} \quad (1)$$

and its value can be given as

$$(m)_{-2} = .. + m_6(-2)^6 + m_5(-2)^5 + m_4(-2)^4 + m_3(-2)^3 + m_2(-2)^2 + m_1(-2)^1 + m_0(-2)^0 \quad (2)$$

Negabinary math shows a couple of ideal conditions over standard combined calculating in multi-operand extension, which makes it significant in explicit explanation applications as mechanized filtering. Negabinary may in like manner find application in execution of complex math reliant on the possibility of whimsical radix number systems. Regardless, it is settled in that, for an extensively helpful application, the math units for the negabinary numbers are more amazing than the equal structure.

A fundamental model is the extension action. The matched development of two numbers needs only one pass on, while two passes on (one positive and the second negative to the accompanying basic position or the two passes on positive, everybody being sent to two dynamic positions) are basic in -2 base. As of late, it has been exhibited that the negative development of two negabinary numbers requires only one pass on, and the method of reasoning capacities with regards to such a negative snake and the contrasting pass on look-ahead terms for brisk extension are no more staggering than combined development.

The closeness between the two assignments gives two complementary techniques for exchanging adders of the two bases. These relations are also seemed to give four changed computations to number change beginning with one base then onto the following.

Let M be an n -bit negabinary number represented as

$$M = m_{n-1}m_{n-2}m_{n-3}.....m_2m_1m_0 \quad (3)$$

$$\text{Its value can be given as} \quad (4)$$

Where

$$M_k \in (0,1) \text{ and } 0 \leq k \leq n-1 \quad (5)$$

For getting the summation of even and odd terms the even and odd bit position are separated. By adding subtracting a term $m_i (2)^k$ (Where m'_k is complement of m_k) and by reduction of terms leadsto

$$\begin{aligned} \text{Defining} \\ m''_k &= m_k \text{ for } k = \text{even} \\ &= m'_k \text{ for } k = \text{odd} \end{aligned} \quad (7)$$

and let

$$Z = \text{---} \quad (8)$$

Substituting (7) and (8) into (6) gives

$$M = \text{---} \quad (9)$$

It might be noticed that M is a negabinary number and the two summation terms on the correct side of the condition (9) are basically numbers in 2 base. M progressively advantageous structure is acquired by speaking

to the summation term by $[M^*]_2$ and this gives

$$M = [M^*]_2$$

where

$$(10a) [M^*]_2 = (10b)$$

A reciprocal connection of equivalent significance can be gotten by using $\sum_{k=0}^i m_k$ as summation term for expansion and deduction to connection (10b) and a comparable rearrangements is given as

$$M = - [M^{**}]_2$$

$$\text{with } [M^{**}]_2 = (11a) (11b)$$

$$m^{**} = m_k \quad \text{for } i = \text{even}$$

$$= m_k \quad \text{for } i = \text{odd}$$

$$(12)$$

with $[]$ representing the largest integer not greater than .

4. Power Dissipation Consideration

The issue of intensity scattering has joined the conventional VLSI requirements of throughput and region. In spite of the fact that this has been to a great extent propelled by the development of convenient and remote registering where preserving vitality is significant due to battery restrictions, power use is additionally an issue in non-compact applications in light of bundling costs, circuit dependability, and cooling contemplations.

The primary wellspring of intensity scattering in very much structured CMOS circuits is the charging and releasing of hub capacitances. The force scattered by a CMOS Gate is given by

Where is the normal exchanging recurrence, B is the physical capacitance, and is the voltage? Transport capacitance can be broad when going off-chip. In the data path, number-number-crunching modules are legitimately the focal wellspring of intensity scattering, yet on-chip interconnect capacitance is transforming into an Issue for significant submicron structures.

Vitality utilization by bus can be limited by diminishing blends of the elements in Eq. (14). Diminished swing voltage methods can be applied to bring down V, and fragmented bus can bring down successful capacitance. In this paper, vitality sparing is endeavored by choosing number portrayals which diminish the exchanging movement comparing to the lines of the information transports. Transport encoding is a significant method for sparing force when going off-chip, and is deserving of assessment for profound submicron innovation and framework on-a-chip structures.

5. The Design

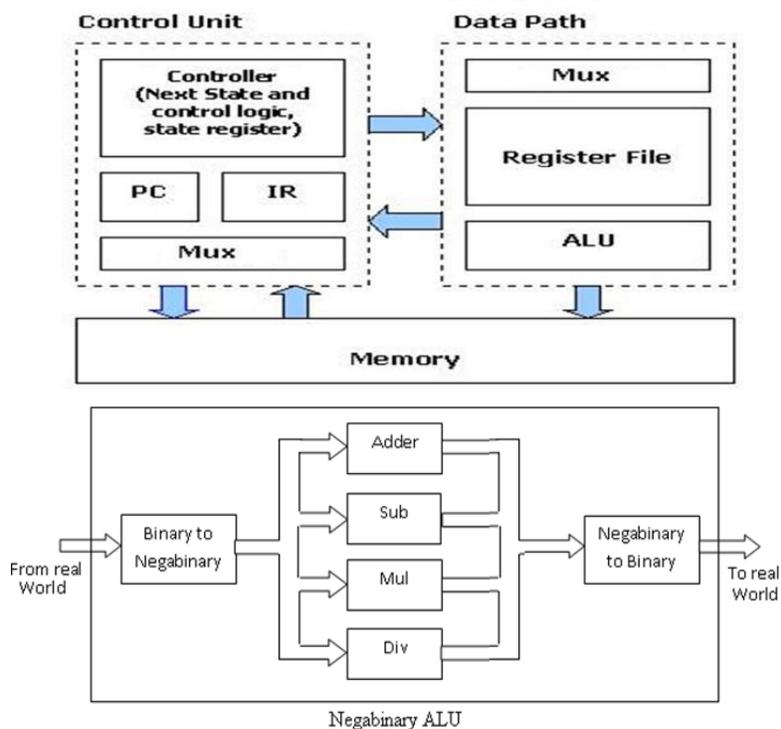


Figure 1. Memory unit

number	bit	carry
-2	0	1 (subtraction.)
-1	1	1
0	0	0
1	1	0
2	0	-1
3	1	-1 (addition.)

Table.1. Arithmetic Operations

While performing the arithmetic operations the above table should be referred for the exact calculation for the addition and subtraction.

6. Simulation Results

6.1 Adder

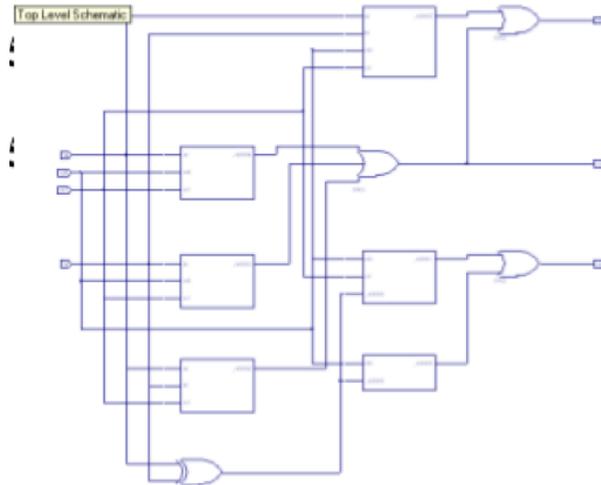


Figure.2. Adder internal structure

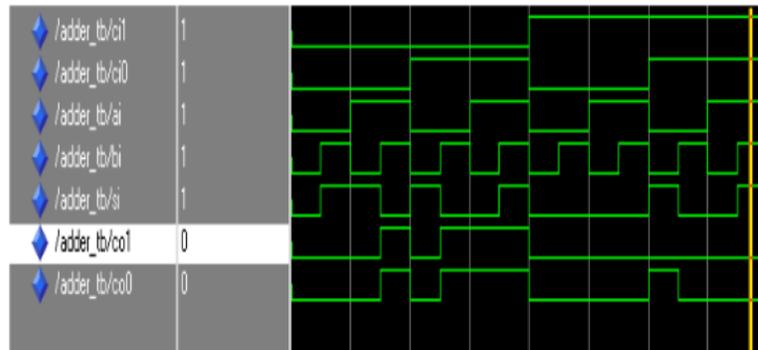


Figure.3. Adder Simulation results

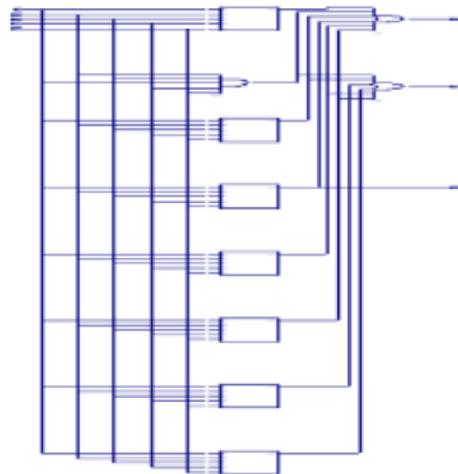


Figure.4. Subtract internal structure

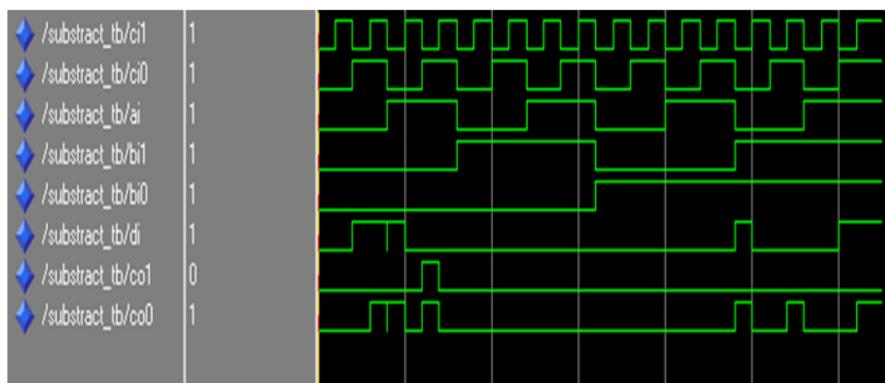


Figure.5. Subtract Simulation results

7. Conclusion

By comparing the above results with the normal two's complement format and taking the heat dissipation in consideration, we can state that that the Negabinary system is fast and will dissipate the less heat.

References

- [1] R. Mehra, S. Jaiswal, H. K. Dixit, "Optical computing with semiconductor optical amplifiers," *Opt. Eng.* Vol. 51, (2012)080901-1.
- [2] K. Song and L. Yan, "Design and implementation of the one-step MSD adder of optical computer," *Appl. Opt.* vol. 51 (2012) pp.917-926.
- [3] A. K. Gosh, A. Bhattacharya, M. Raul, A. Basuray, "Trinary arithmetic and logic unit (TALU) using savart plate and spatial light modulator (SLM) suitable for optical computation in multivalued logic," *Opt. Las.Tech.* vol. 44 (2012) pp. 1583-1592.
- [4] D. K. Gayen, J. N. Roy, C. Taraphdar, and R. K. Pal, "All-optical reconfigurable logic operations with the help of terahertz optical asymmetric demultiplexer," *Optik* vol. 122 (2011) pp.711-718.
- [5] J. P. Sokoloff, P. R. Prucnal, I. Glesk, M. Kane, "A terahertz optical asymmetric demultiplexer (TOAD)," *IEEE Photo. Techn. Let.* Vol. 5 (1993) pp. 787-790.
- [6] K. E. Stubkjaer, "Semiconductor optical amplifier-based all optical gates for high-speed optical processing," *IEEE J. Sel. Top. Quantum Electron* vol. 6 (2000) pp.1428-1435.
- [7] A. Sharaiha, J. Topomondzo, P. Morel, "All-optical logic AND-NOR gate with three inputs based on cross-gain modulation in a semiconductor optical amplifier," *Opt. Commun.* Vol. 265 (2006) pp.322-325.
- [8] D. K. Gayed, J. N. Roy, "All-optical arithmetic unit with the help of terahertz- optical-asymmetric-demultiplexer-based tree architecture," *Appl. Opt.* vol. 47 (2008) pp.933-943.
- [9] J. N. Roy, D. K. Gayen, "Integrated all-optical logic and arithmetic operations with the help of a TOAD-based interferometer devicealternative approach," *Appl. Opt.* vol. 46 (2007) pp.5304-5310.
- [10] J. Y. Kim, S. K. Han, S. Lee, "All-optical multiple logic gates using parallel TOAD structures," *IEEE Las. and Electro. Optics Society annual meeting* (2005) pp.133-134.
- [11] G. Li, L. Liu, L. Shao, Z. Wang, "Negative binary arithmetic algorithms for digital parallel optical computation," *Opt. Let.* Vol. 19 (1994) pp.1337-1339.
- [12] A. K. Cherri, H. A. Kamal, "Efficient optical negabinary modified signed- digit arithmetic: one-step addition and subtraction algorithms," *Opt. Eng.* vol. 43 (2004) pp.420-425.

- [13] A. K. Cherri, "All-optical negabinary adders using Mach-Zehnder interferometer," *Opt. Las. Techn.* vol. 43 (2011) pp.194-203.
- [14] Moon Banerjee et.al Morphological Analysis of Fibre Reinforced Laminate Made By Hand Lay-Up Process, *International Journal of Innovative Technology & Exploring Engineering*, ISSN:2278–3075 (Online), Volume-9 Issue-3, January 2020, Page No.434-437.
- [15] Moon Banerjee et.al Experimental and numerical analysis of extrusion process for AA 7178 alloy with varying process parameters; *Materials Today Proceedings*; Vol:- 5, Issue:-2, Part:-2, 2018, Pages6839-6847.
- [16] Mohan Awasthy et.al Q Learning Based Technique for Accelerated Computing on Multicore Processor *IJCSE* Vol 8 No.5 601-607 ISSN:0976 a. 5166 Oct – Nov 2017
- [17] Mohan Awasthy et.al Synchronous Q Learning Based Technique for Performance Improvement in Multi Core Processor" *International Journal of Technology* Vol. 8 Issue 2) July – December 2018 pp634-641.
- [18] Manish Pandey et.al "Study & Scheme Of Neuro-Fuzzy System With Various Databases for Emotional States Recognition *International Journal of Advanced Science and Technology* I SSN: 2005-4238 Vol. 29, No. 7, (2020), pp. 804-810
- [19] Mohan Awasthy et.al "Power Transmission through Solar Power Satellite to Earth Surface with Minimum Power Loss" *International Journal of Engineering and Advanced Technology (IJEAT)* ISSN:2249–8958, Volume-8 Issue-6, August 2019 pp 845-850
- [20] Mohan Awasthy et.al "Mobile Robot Path Planning using Weight Grid Algorithm" *International Journal of Control and Automation* ISSN: 2005-4297 Vol. 13, No. 1, (2020), pp. 477 –484
- [22] Mohan Awasthy et.al "Design And Analysis Of Mutual Inductance Based Wireless Power Transfer (WPT) System Suitable For Powering Solar Power Satellite (SPS)" *International Journal of Advanced Science and Technology* ISSN: 2005-4238 Vol. 29, No. 12s, (2020), pp. 941-952
- [23] [[22] Rajesh Tiwari et.al "Dynamic Load Distribution To Improve Speedup Of Multi-Core System Using MPI With Virtualization" *International Journal of Advanced Science and Technology* ISSN: 2005-4238 Vol. 29, No. 12s, (2020), pp.931-940
- [24] Mohan Awasthy et.al "Critical Review and Assessment of Space Based Solar Power Satellite (SBSPS)" *Test Engineering and Management* May - June 2020 ISSN: 0193-4120 pp 11322 -11336
- [25] Manish Pandey et.al "Review, Study & Modelling Of Neuro-Fuzzy System, It's Performance Comparison Using Various Speech Databases For Recognition Of Emotional States" *Journal of Critical Reviews* ISSN-2394-5125 Vol 7, Issue 12, 2020 pp1231-1240
- [26] Manish Kumar and Vinay Kumar Deolia, "Performance Analysis of Low Power LNA using Particle Swarm Optimization for wide band Application", Vol. 111, pp.152897, *International Journal of Electronics and Communication*, Elsevier,