European Journal of Molecular & Clinical Medicine
ISSN 2515-8260 Volume 7, Issue 4, 2020

Design and Simulation of Heterogeneous Adder Using Xilinx Vivado

[1]Manish Kumar, [2]Abhay Chaturvedi
[1,2]Department of Electronics and Communication, GLA University, Mathura, UP, India.
manish.kumar@gla.ac.in, abhay.chaturvedi@gla.ac.in

Abstract
The adders are logic circuits designed to execute "high speed Arithmetic operations" in Arithmetic Logic Unit (ALU) utilized in processors. The basic Adders are "Half Adder and Full adder". The diverse kinds of adders are Carry Look ahead Adder (CLA), Ripple Carry Adder(RCA), Carry Select Adder (CSLA), &Carry Skip Adder(CSKA). In this manuscript, Heterogeneous adder (HA) architecture is designed with support of diverse Homogeneous adders and Heterogeneous adders are contrasted with Homogeneous adders in terms of power, delay, & area. This architecture is based on a VHDL and compares their performance with Xilinx VIVADO software tool.
Keywords-Adders, RCA, CLA, Simulation, VHDL, Arithmetic Logic Unit (ALU), and Half Adder (HA), Full adder (FA)

1. Introduction

The arithmetic operations perform a significant role in numerous digital systems. The adders are the main modules in Digital signal Processors &Microprocessors. Adders have utilized to execute the Addition of numbers, Multiplication, Subtraction and Division operations. They require low efficient power and area designed technique to increment presentation of circuit. Hence, the area efficient design createssmaller chip size and decreases the price. The dissimilar adders are RCA, CLA, CSLA, & CSKA.
Here Heterogeneous adder means concatenation of different homogeneous adders and Homogeneous adder is the combination of the same type of adders. The designed adder will be contrasted with each other in terms of power &area along with implementation & experimental results utilizing Xilinx VIVADO.

2. Related Work

A. Ripple Carry Adder

The RCA might be designed by "cascading full adder" in series i.e., carry from past FAwill be connected as input carry for next phase. The FAwill be an elementary building block of RCA. Hence, to design n-bit parallel adder, it needs n full adders. The block diagram of RCA will be shown in below figure.

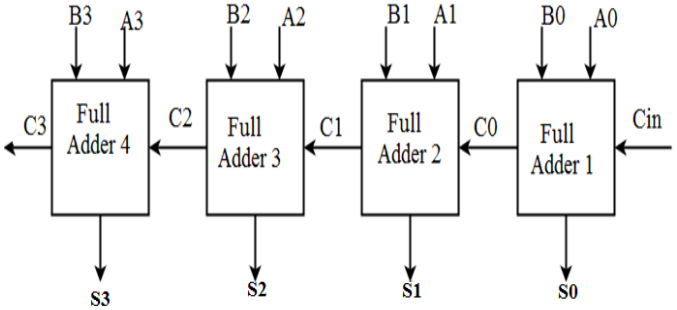

Fig.1: 4-Bit RCA

Example: A=1010; B=0101;Cin =0 are the inputs of the adder than the output is S=1111 with a carry '0'. The main restriction of RCA will be that as the delay & length of bit goes on enhances. Since every FA should wait for carry bit from previous FA. So RCA is relatively slow.

B. Carry Look Ahead Adder

The CLA is also identified as Fastest Adder. It develops speed by decreasing the amount of timeneeded to describe the carry bits. The flow diagram of CLA is displayed below:

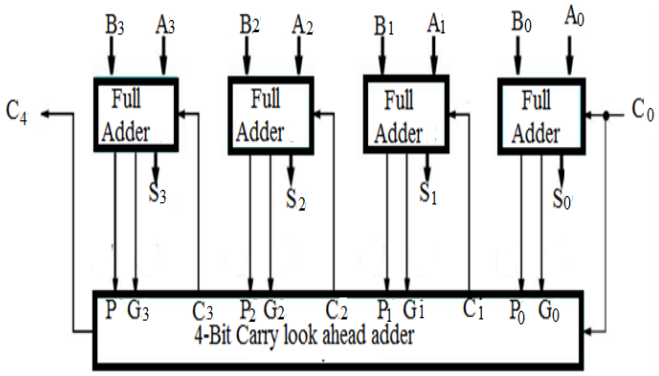

Fig.2: 4-Bit CLA

The CLA estimates one or more carry bits before the sum that decreases wait time to estimate outcome of larger value bits. The CLA working might be understood by "Boolean expressions" dealing with FA and it will be provided by

Carry propagate(Pi) = A xor B
Carry Generate(Gi) = A and B

Both produce and propagate signals based only on input signals, the novel expressions for output sum and carry are

Sum(Si)= Pi xorCi ;
Carryout(Ci+1)=Gi+ Pi Ci

The limitation in CLA is if the bit length goes on increasing the circuit complexity is also increased.

C. Carry Select Adder

The CSLA comprises of multiplexer& 2RCAs. It comprises of an independent generation of sum and carry Cin=0 &Cin=1 have calculated parallel. On the basis of the Cin&external multipliers select the carry to next phase. Moreover, on the basis of carry input the sum is chooses, therefore, the delay will be decreased. The flow diagram of the CSLA will be shown in below figure.

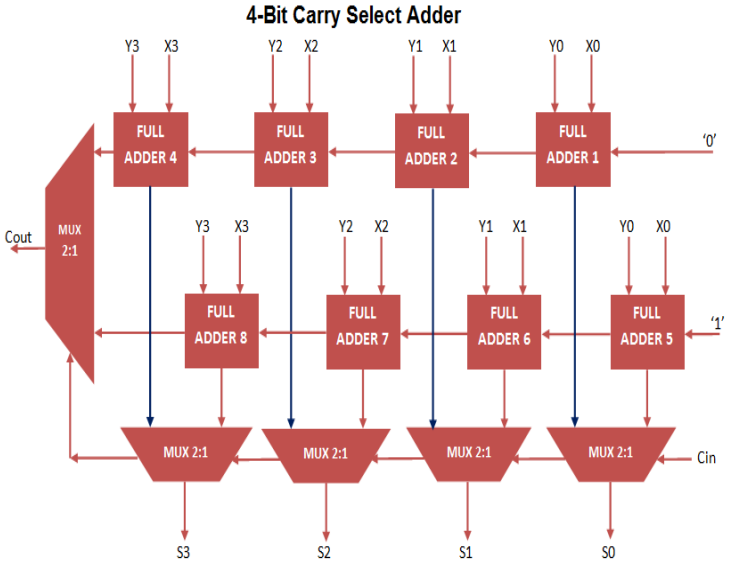

Fig.3: 4-Bit CSLA

D. Carry Skip Adder

The CSKA will be also identified as carry Bypass adder and that enhances on RCA delay. The enhancement of worst delay will be attained by utilizing numerous CSKAs to create a block skip adder.

The skip logic comprises of 1 multiplexer &m-input AND-gate. As propagate signals have contrasted in parallel and available early, the difficult way for skip logic in CSKA comprises only of delay imposed by multiplexer. The flow diagram of CSKA is displayed in below figure.

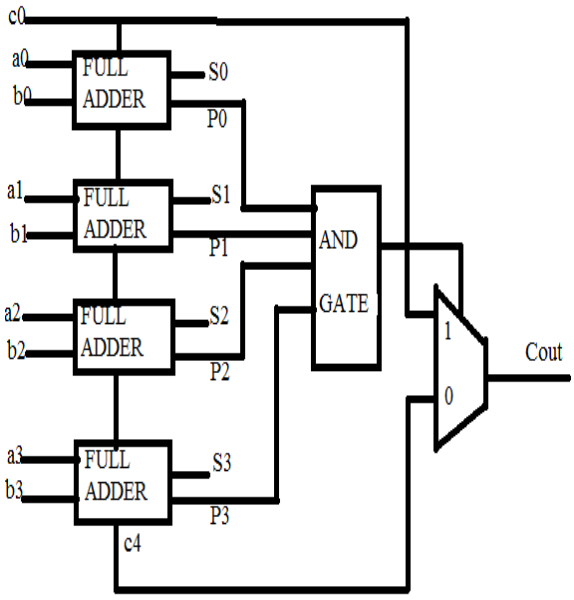

Fig.4: 4-Bit Carry Skip Adder

3. PROPOSED MODEL

The architecture of heterogeneous adder (HA)is suggested &designed with support of diverse architecture of homogeneous adder.

The proposed technique is 16-bit HA and it is concatenation of 8-bit RCA, 8-bit CLA. It will be compared with the 16-bit Homogeneous adder in terms of delay, area, &power.The flow diagram of 16-bit HA is represented in below figure.

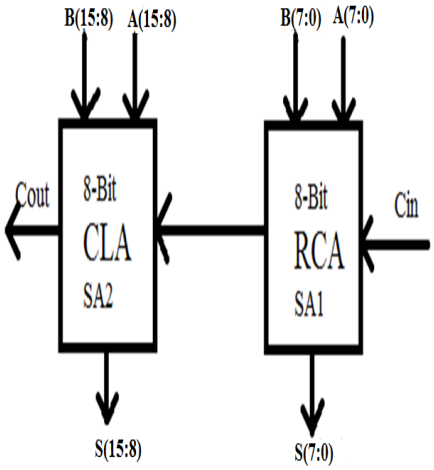

Fig.5: 16-Bit HA

4. RESULTS

1. Experimental Result for Proposed Method
2.

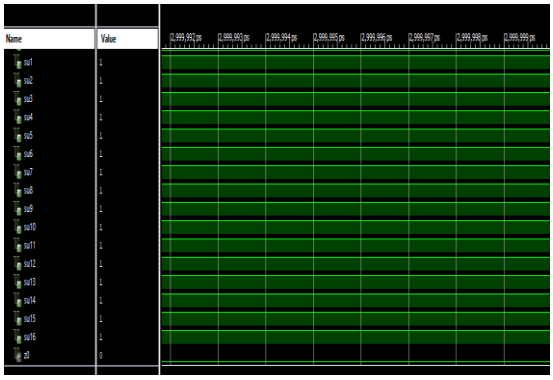

Fig.6: Experimental outcomes of suggested HA

3. Schematic Diagram for Proposed Method
4.

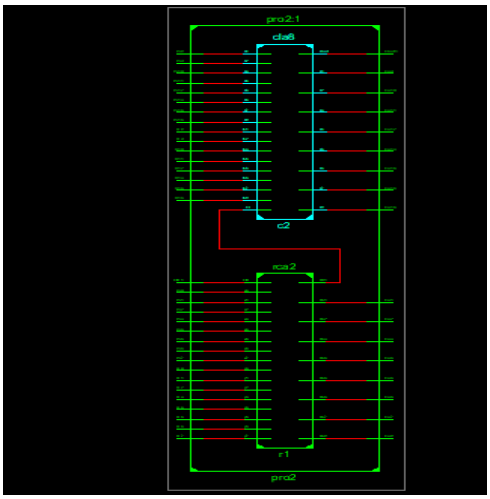

Fig.7: Schematic Diagram for suggested HA

5. Comparison and Tabulation

	8-Bit RCA	8-Bit CLA	Heterogeneous Adder	Homogeneous Adder
Slice LUTs	8	17	25	38
Bonded IOB	25	25	50	50
Utilization %(LUT)	0.01	0.02	0.02	0.02
Utilization %(IO)	8.67	8.67	14.67	16.67

Table 1: Comparison of Utilization among 8-Bit RCA,8-Bit CLA, HA, Homogeneous Adder

	8-Bit RCA	8-Bit CLA	Heterogeneous Adder	Homogeneous Adder
On-chip Memory	5.43w	5.60w	11.07w	12.03w
Junction Temperature	34.6’c	35.6’c	50.3’c	53.6’c
Thermal Margin	64.4’c	49.4’c	43.7’c	44.7’c
Signal (Data)	0.07w	0.17w	0.276w	0.367w
Logic	0.02w	0.05w	0.083w	0.096w
I/O	5.76w	5.28w	10.98w	11.96w

Table 2:Comparison of Power Summary between 8-Bit RCA,8-Bit CLA, HA, Homogeneous Adder

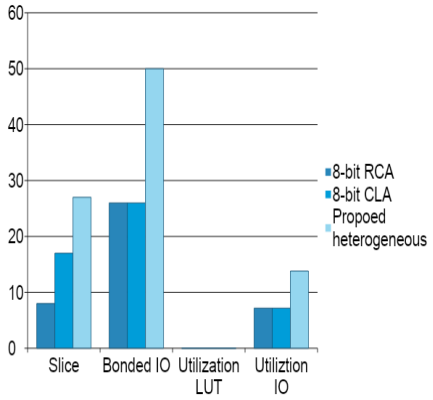

Fig.8: Comparison graph of HA usage

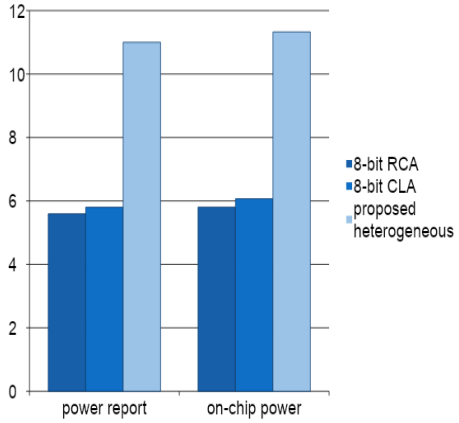

Fig.9: Comparison graph of power consumption in Heterogeneous Adders

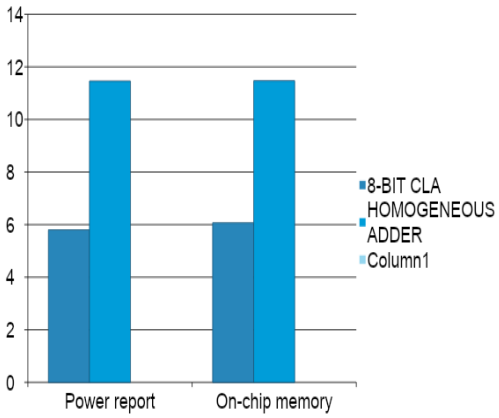

Fig 11: Comparisongraphof powerconsumptionin homogenous adder

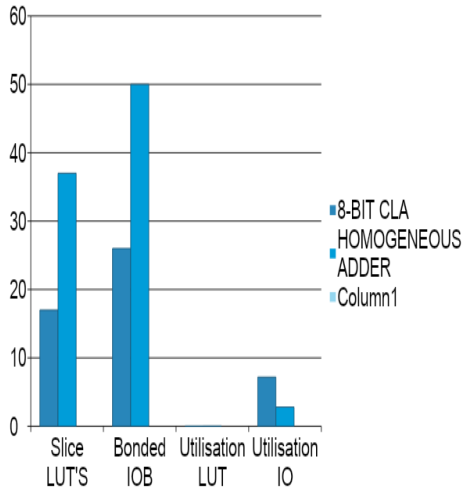

Fig.10: Comparison Graph of Utilization of Homogeneous Adder

6. Conclusion

This manuscript suggests the HA with the use of 8-Bit RCA &8-Bit CLA and simulation as stated by its properties utilizing VHDL in VIVADO. This method has low thermalmargin under consumption of power. It has minimum delay &area that provesto be simple answer in developing speed of adder circuit. The relevant usage &powersummary of suggested method 16-Bit HA &16-Bit Homogeneous adder wascompared with the use of Bar- Graph.

7. References

[1] Rajender Kumar, Sandeep Dahiya, "Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL Environment," International Journal of Engineering Science and Innovative Technology (IJESIT), vol. 2, no. 4, July 2013.

[2] Aishwarya T, Arvind Prasad L, Nikith G S, Ahish S, "FPGA Implementation of Optimized Heterogeneous Adder for DSP Applications," International Journal of Engineering Research & Technology (IJERT), vol. 3, no. 5, May 2014.

[3] K.Gowthami, Y.Yamini Devi, "Design of 16-bit Heterogeneous Adder Architectures Using Different Homogeneous Adders," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 5, no. 10, October 2016.

[4] Y. T. Pai and Y. K. Chen, “The fastest carry-lookaheadadder,” Proceedings of the second IEEE international workshop on Electronic design test and applications, 2004.

[5] Rajender Kumar, Sandeep Dahiya, "Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL Environment," International Journal of Engineering Science and Innovative Technology (IJESIT), vol. 2, no. 4, July 2013.

[6] Aishwarya T, Arvind Prasad L, Nikith G S, Ahish S, "FPGA Implementation of Optimized Heterogeneous Adder for DSP Applications," International Journal of Engineering Research & Technology (IJERT), vol. 3, no. 5, May 2014.

[7] Nagaraj Y, Shrinivas K, Veeresh K, Veeresh A, MadhuPatil and Dr. Chirag Sharma, "FPGA implementation of different adder architectures," International Journal of Emerging Technology and Advanced Engineering, vol. 2, no. 8, pp. 362-364, August 2012.

[8] RaminderPreet Pal Singh, Ashish Chaturvedi, Onkar Singh, "Trade-offs in Designing High-Performance Digital Adder based on Heterogeneous Architecture," International Journal of Computer Applications (0975 – 8887), vol. 56, no. 13, October 2012.

[9] Y. T. Pai and Y. K. Chen, "The fastest carry-lookahead adder," Proceedings of the second IEEE International Workshop on Electronic Design Test and Applications (DELTA), 2004.
[10] K.Gowthami, Y.Yamini Devi, "Design of 16-bit Heterogeneous Adder Architectures Using Different Homogeneous Adders," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 5, no. 10, October 2016.
[11] Neha Agarwal and Satyajit Anand, "Logical Effort to Study the Performance of 32-bit Heterogeneous Adder," International Journal of Computer Applications, vol. 65-No.16, March 2013
[12] Manish Kumar andVinay Kumar Deolia, “Performance Analysis of Low Power LNA using Particle Swarm Optimization for wide band Application”, Vol. 111, pp.152897, International Journal of Electronics and Communication, Elsevier, 2019.
[13] Vishal Goyal, Puneet Mishra, Vinay Kumar Deolia, “A Robust Fractional Order Parallel Control Structure for Flow Control using a Pneumatic Control Valve with Nonlinear and Uncertain Dynamics” Arabian Journal for Science and Engineering ,
[14] Aasheesh Shukla, Vishal Goyal, Manish Kumar, Vinay kumarDeolia, and Munesh Chandra Trivedi “MMSE based beam former in Massive MIMO IDMA downlink systems”, Journal of Electrical Engineering.71(1), march 2020